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Mobile Virtual Synchronous Machine for Vehicle-to-Grid Applications

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Abstract

The Mobile Virtual Synchronous Machine (VISMA) is a power electronics device for Vehicle to Grid (V2G) applications which behaves like an electromechanical synchronous machine and offers the same beneficial properties to the power network, increasing the inertia in the system, stabilizing the grid voltage, and providing a short-circuit current in case of grid faults. The VISMA performs a real-time simulation of a synchronous machine and calculates the phase currents that an electromagnetic synchronous machine would produce under the same local grid conditions. An inverter with a current controller feeds the currents calculated by the VISMA into the grid.

In this dissertation, the requirements for a machine model suitable for the Mobile VISMA are set, and a mathematical model suitable for use in the VISMA algorithm is found and tested in a custom-designed simulation environment prior to implementation on the Mobile VISMA hardware. A new hardware architecture for the Mobile VISMA based on microcontroller and FPGA technologies is presented, and experimental hardware is designed, implemented, and tested. The new architecture is designed in such a way that allows reducing the size and cost of the VISMA, making it suitable for installation in an electric vehicle.

A simulation model of the inverter hardware and hysteresis current controller is created, and the simulations are verified with various experiments. The verified model is then used to design a new type of PWM-based current controller for the Mobile VISMA. The performance of the hysteresis- and PWM-based current controllers is evaluated and compared for different operational modes of the VISMA and configurations of the inverter hardware.

Finally, the behavior of the VISMA during power network faults is examined. A desired behavior of the VISMA during network faults is defined, and experiments are performed which verify that the VISMA, inverter hardware, and current controllers are capable of supporting this behavior.

Kurzfassung

Die mobile Virtuelle Synchronmachine (VISMA) ist eine leistungselektronische Komponente für Vehicle to Grid (V2G) Anwendungen, die sich wie eine elektromechanische Synchronmaschine verhält und damit zusätzliche Netzdienstleistungen erbringt, wie die Erhöhung der Trägheit im System, Momentanreserve, die Stabilisierung der Netzspannung und die Bereitstellung eines Kurzschlussstromes bei Netzstörungen. Die VISMA führt eine Echtzeitsimulation einer Synchronmaschine durch und berechnet die Phasenströme, die eine elektromagnetische Synchronmaschine unter den gleichen lokalen Netzbedienungen erzeugen würde. Ein Umrichter mit einem Stromregler speist die durch die VISMA berechnete Sollströme ins Netz.

In dieser Dissertation werden die Anforderungen für ein Maschinenmodell zur Beschreibung der mobilen VISMA dargelegt. Dazu wird ein mathematisches Modell für den Einsatz im VISMA-Algorithmus erarbeitet und vor der Implementierung auf der Mobilen VISMA Hardware in einer speziell dafür entwickelten Simulationsumgebung getestet. Eine neue, auf Mikrocontroller und FPGA-Technologien basierte, Hardware-Architektur für die Mobile VISMA wird vorgestellt und eine experimentelle Hardware entwickelt und getestet. Die neue Architektur wird derart konzipiert, dass Größe und Kosten der VISMA verringert werden können, was den Einbau der VISMA in ein Elektrofahrzeug ermöglicht.

Ein Simulationsmodell des Wechselrichters mit einem Phasenstromregler wird entworfen und die Simulationen mit verschiedenen Experimenten verifiziert. Das verifizierte Modell wird verwendet, um einen neuartigen PWM-basierten Stromregler für die Mobile VISMA zu entwickeln. Die Eigenschaften der Hysterese- und PWM-basierten Stromregler werden für verschiedene Betriebsarten der VISMA und für verschiedene Konfigurationen des Wechselrichters untersucht und verglichen.

Schließlich wird das Verhalten der VISMA während Stromnetzstörungen untersucht. Das gewünschte Verhalten der VISMA während Netzstörungen wird definiert und experimentell verifiziert.

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Contents

Chapter 1

Introduction

1.1 Motivation

The power distribution system was originally developed using a top-down architecture, where large central generators are responsible for generating most of the power. In this architecture, the flow of power is unidirectional, from the producer to the consumers, and the grid operator is responsible for maintaining power quality throughout the grid. With the deregulation of energy markets and a growing penetration of renewable energy resources, the architecture of the grid has been changing to what is known as a distributed grid. In a distributed grid, there are many small-scale generation facilities, e.g. combined heat and power plants, wind turbines, and solar generators, which vary in size and output power. The principle of power generation in centralized and distributed grids differs significantly, which has consequences on both power quality and grid stability. Whereas large power plants almost exclusively use synchronous machines for power generation, distributed generators often use other generation principles and must be coupled to the grid through grid-tie inverters.

In the coming years, we can foresee a substantial growth in the electric vehicle market, which will influence electric power usage, and, in effect, the power distribution network. Figure 1.1 shows the architecture of a power network with a high penetration of distributed generators using renewable energies (solar, wind) and electric vehicles connected to the grid.

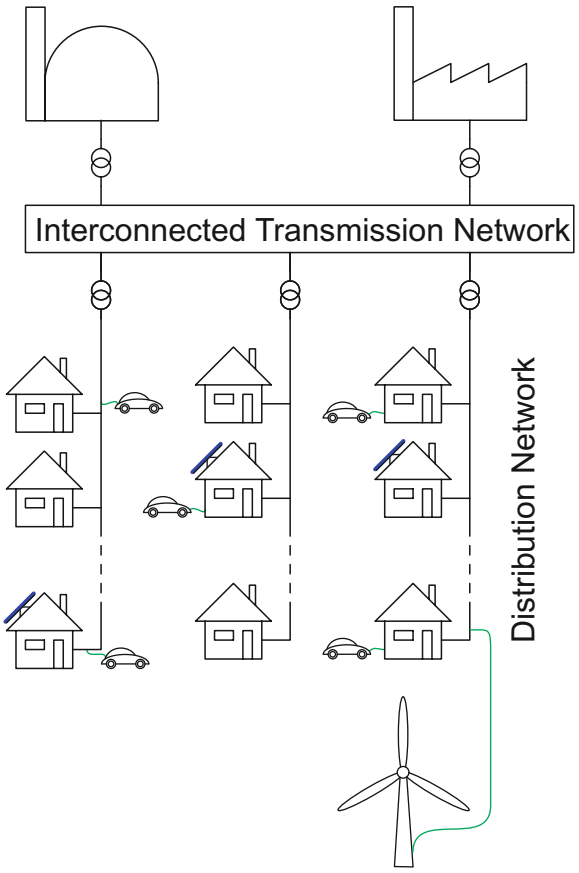


FIGURE 1.1: Architecture of electrical power network with high penetration of distributed generators using renewable energy resources (solar, wind) and electric vehicles

In power generating facilities using synchronous generators, kinetic energy is stored in the rotating mass of the rotor and turbines. This kinetic energy is useful when an unbalance occurs between generation and demand, as the inertia limits the rate of change of frequency of the grid voltage. With a greater penetration of inverter-coupled generating facilities in the power network, the total inertia in the system decreases, which can cause dynamic stability problems. One way to increase the inertia in a power system is to add kinetic energy storage directly, e.g. using flywheel technology, as was suggested in [1]. This concept involves installing synchronous machines coupled with a flywheel in the power network. The problem with this method is the additional cost of installing and maintaining the flywheel system.

At the Institute of Electrical Power Engineering (IEE) of the Clausthal University of Technology, a control concept for a power inverter was invented by Ralf Hesse, which allows the inverter to behave like a synchronous machine, and, like a real

synchronous machine, increase the system inertia and provide other features beneficial to grid stability and power quality [2, 3]. The system developed by Hesse is known as a Virtual Synchronous Machine (VISMA). The VISMA performs a real-time simulation of a synchronous machine where the grid voltage is measured and the phase currents that an electromagnetic synchronous machine would produce under the same grid conditions are calculated. A current-controlled inverter then feeds these currents into the grid. With the VISMA, the inverter used by the distributed generator for feeding power into the grid improves grid stability.

Concepts similar to the VISMA have been gaining in popularity recently, and there are several projects worldwide which try to equip inverters with synchronous machine properties in order to increase inertia in the grid and improve grid stability. One of these projects is the Virtual synchronous machines for frequency stabilization in future grids with a significant share of decentralized generation (VSYNC) project [4–9]. The goal of the VSYNC project is to provide virtual rotational inertia to distributed generators by equipping them with intelligent grid-tie inverters with short-term energy storage, allowing them to operate like Virtual Synchronous Generators (VSGs), which, for short time intervals, exhibit some of the desired properties of synchronous machines [8] and contribute to the stabilization of grid frequencies caused by large load fluctuations in the grid [4]. There are two test sites for the VSYNC project, one in the Netherlands with ten 5 kW, single-phase VSGs, and one in Romania with a 100 kW VSG [8].

The power exchange equation of a VSG is given as [5]:

$$P_m = \omega_g \cdot J \cdot \left(\frac{d}{dt} \omega_g(t) \right) \tag{1.1}$$

Where P_m is the mechanical power needed to accelerate the rotating mass with an inertia J, and is equal to the electrical power drawn from the grid by the VSG, and ω_g is the grid frequency. The VSG therefore only models the inertia of a synchronous machine, but does not consider other synchronous machine properties. The VSG feeds power into the grid using a PWM-controlled inverter [8].

Another concept similar to the VISMA is that of the synchronverter [10] conceived by researchers from the UK and Israel. The synchronverter also performs a real-time simulation of a synchronous machine. Unlike the VISMA, which measures the

voltages at the Point of Common Coupling (PCC) with the grid and outputs currents, the synchronverter measures the phase currents and uses a PWM-controlled inverter to output voltages equal to the back-Electromotive Forces (EMFs) that a synchronous machine would produce under the same conditions on the grid. The synchronverter synchronous machine model does not include damper windings. Instead, damping in the system is implemented as mechanical damping. Also, the synchronverter machine model assumes that the input to the machine's field winding is a current and not a voltage, simplifying the machine equations. The VISMA, on the other hand, uses a more complex model of the synchronous machine which includes damper windings and voltage input to the field winding. This allows the control of the VISMA as if it were an electromechanical synchronous machine.

Recently a research team from Canada proposed its model of a virtual synchronous machine [11], where the synchronous machine is modeled as a damping and synchronizing torque which are proportional to the rotor speed deviation and rotor angle deviation, respectively. Another team from Japan is investigating VSGs [12] based on VSYNC VSGs [5] expanded to include damping that models the synchronous machine's damper windings.

Compared to the alternatives to the VISMA presented here, which only have a part of the static and dynamic properties of a synchronous machine, the VISMA possesses the complete static and dynamic properties of a synchronous machine [13]. The machine model foreseen by the VISMA concept most closely represents an electromechanical synchronous machine, and the well-known and tested control concepts for electromechanical synchronous machines can be transferred directly to the VISMA.

The concept of the Mobile VISMA arose with the realization that the VISMA can be used for Vehicle to Grid (V2G) applications. A V2G system is a system where a plug-in electric vehicle is used to support the power network when plugged in for charging. Plug-in electric vehicles have energy storage capacity in their batteries, which has many potential applications. The support to the grid offered by electric vehicles may involve the provision of ancillary services e.g. frequency regulation or spinning reserve as well as peak load shaving and reactive power support. Without using some form of smart charging, a growing penetration of electric vehicles can have a negative effect on the power grid, because of the vehicles' high-consumption of electric energy. Uncoordinated charging may increase the power losses in the distribution grid and lead to voltage deviations, which may be unacceptably high,

especially during the evening peak [14]. V2G systems can be classified into unidirectional V2G systems [15, 16] (also known as V1G), where the vehicle supports the grid while drawing power to charge the battery, and bidirectional systems, where the vehicle can feed power back into the grid. There are numerous V2G concepts proposed in literature. An overview of some these concepts and an analysis of the profitability of different V2G scenarios with consideration of the effect on battery life can be found in [17].

In the power network energy cannot be stored, and supply and demand must be matched at all times. If supply is greater than demand, an increase in the frequency of the grid voltage can be observed. If supply is smaller than demand, the frequency decreases. One of the problems with renewable energy resources such as wind and solar is that they are non-dispatchable in the traditional sense, i.e. their output power cannot be adjusted to match demand. Their output power depends on weather conditions and can be calculated a day ahead using simulation and prognoses, but it cannot be regulated. The intermittent nature of wind and solar power and the high cost of creating electrical energy storage facilities is one of the main problems for the realization of a reliable power network based on renewable energies. Using V2G technologies, the reliability of power networks with a high penetration of renewable generation can be improved.

The VISMA allows bidirectional transfer of power between the grid and the battery. It can be operated in generator mode, supplying power to the grid, or in motor mode, drawing power from the grid. In the stationary VISMA developed at the IEE, it was assumed that the VISMA would be connected to a renewable energy generator, e.g. solar or wind generator. The VISMA would by default run in generator mode, feeding power into the grid. The mobile VISMA on the other hand is designed to be integrated in electric vehicles, which, with the exception of plug-in hybrid vehicles and vehicles with range extenders, are not equipped with power generating capability and are net consumers of electrical energy. From the vehicle owners point of view, connecting the vehicle to the grid is done to charge the on-board batteries. Any grid stabilizing services which the mobile VISMA may provide should not interfere with this objective and should not lead to a deterioration of the lifespan of the batteries.

In electric vehicles, the most popular batteries used are lithium-ion batteries due to their high energy density. The cycle life of a battery is the number of charge-discharge cycles until its nominal capacity drops below 80% of the initial capacity.

Although the battery may still be usable afterwards, the resulting decrease in the driving range may not be acceptable to the vehicle owner. The deeper the a lithium-ion battery is discharged, the faster its capacity deteriorates. The relationship between the Depth of Discharge (DOD) and the number of charge/discharge cycles for lithium-ion batteries is strongly non-linear, and the cost of storage of energy in the battery in €/kWh decreases significantly for shallow discharge [17]. With the current price of batteries for electric vehicles, using a Mobile VISMA operated in generator mode for services such as peak shaving may not be feasible, but offsetting peak demand can still be accomplished by throttling the charging rate without affecting the battery lifespan. Used in motor mode to charge an electrical vehicle's batteries, the VISMA also has properties beneficial to the grid which include increasing the inertia in the power network and voltage stabilization [18].

1.2 Dissertation Goals and Structure

Three problems are tackled in this dissertation. The first problem is how to create a VISMA system which can be installed in a passenger car, which is a design optimization and system integration problem. The second problem is to design a current controller for the VISMA which will allow feeding in of the currents calculated by the VISMA into the grid with the minimum tracking error. The final problem is to verify the behavior of the VISMA and the current controller during faults in the power network.

The structure of this dissertation is as follows. In Chapter 2 a mathematical model of the synchronous machine is presented which can be used in the VISMA algorithm. In Chapter 3 the design of the Mobile VISMA hardware is discussed. Chapter 4 introduces a simulation model of the Mobile VISMA inverter and hysteresis current controller, and the validity of the simulation model is verified with experiments. In Chapter 5 the developed simulation model is used to design a PWM-based controller for the VISMA. Next, the performance of the PWM-based and hysteresis current controllers is compared in Chapter 6. Chapter 7 examines the behavior of the VISMA and current controllers during power network faults. The results of this dissertation are summarized in Chapter 8.

Chapter 2

VISMA Synchronous Machine Model

This chapter deals with the mathematical model of the synchronous machine that can be simulated on a microcontroller platform in real time. The requirements for the mathematical model of the synchronous machine are introduced, and a brief history of the VISMA is provided with focus on machine model implementation issues. A machine model which is suitable for the Mobile VISMA is introduced and numerical methods for simulation are discussed.

2.1 Machine Model Requirements and Implementation History

There are numerous ways to set up the mathematical equations which describe the behavior of a synchronous machine. For the simulation model used in the VISMA the inputs to the system are the three phase voltages measured at the PCC with the grid, a virtual exciter voltage, and a virtual mechanical torque. The outputs of the simulation are the desired phase currents.

A mathematical model is needed which can be used in a real-time simulation of the machine. This puts limits on the type of solver used for solving the differential equations describing the synchronous machine. The solver should be computationally simple, preferably Euler, to facilitate implementation on a low-cost

microcontroller. State-of-the-art microcontrollers used for industrial applications have 32-bit Central Processing Units (CPUs) and Floating Point Units (FPUs) which can handle single-precision (32-bit) floating point numbers, so the simulation should be stable with single-precision floating point variables.

The original VISMA [3] developed at the IEE of the Clausthal University of Technology was implemented on a dSpace rapid prototyping system. The dSpace system allows the graphical modeling of processes using Matlab/Simulink and automatic code generation for dSpace real-time hardware. The machine model was implemented as a block diagram in Simulink, and code for the dSpace system was automatically generated from the Simulink model. The problem with this approach is its lack of transparency. Although the generated code can be successfully executed on the dSpace system, the internal structure of the code remains unknown. The code generated from Simulink can be viewed, but the legibility of the code is poor. Until now, well written manual code can be more efficient than automatically generated code, and it gives the designer more control over the structure and execution sequence of the program.

The first attempt to implement the VISMA on a microcontroller was the Mini VISMA [19]. The program code for the Mini VISMA was written in C and implemented on an Infineon Tricore TC1796 microcontroller [20]. The mathematical model of the synchronous machine used in the Mini VISMA came from the original VISMA as described in [3], and the Mini VISMA used the Euler integration method for solving the machine differential equations.

Two problems were found with the synchronous machine model used in the original and Mini VISMAs. Firstly, the model was not stable when the measured grid voltages were not ideal sine waves or if there was noise present in the measured voltages. The engineers working on the Mini VISMA circumvented this problem by using ideal sine waves as input voltages to the synchronous machine model. These ideal sine waves were obtained using a Phase-locked Loop (PLL) synchronized with the grid voltage. The disadvantage of this method is that some of the dynamic properties of the synchronous machine are lost, as the machine can no longer quickly react to changes in the grid voltage or frequency.

The second problem with the original machine model was that the simulation proved to be stable only if double-precision (64-bit) floating point variables were used in the simulation model. Like most 32-bit microcontrollers, the TC1796

microcontroller used in the Mini VISMA does not have a double-precision FPU, without which mathematical operations on double-precision floating point numbers are time consuming. In the Mini VISMA, the execution of the real-time simulation with a frequency of 10 kHz uses the microprocessor almost to capacity, leaving little time for other tasks.

There is ongoing research at the IEE and Lower Saxony Energy Research Center (EFZN) to improve the machine model used for the VISMA. To check whether a VISMA machine model would be suitable for microcontroller implementation, I created a synchronous machine simulation platform in the C# programming language, where the synchronous machine can be simulated using different solver methods (e.g. Euler, Runge-Kutta) and using variables with different number formats (e.g. single- and double-precision floating point numbers and fixed point numbers). Using recorded grid voltages as inputs, simulations can be performed to evaluate the stability of a machine model for a given solver method and number format. Since the code used for the simulations is written in C#, which has high similarity to C, the VISMA mathematical model and simulation code can easily be ported to C for implementation on a microcontroller.

One synchronous machine model tested by IEE researchers on a dSpace system showed stability with real, measured grid voltages, and does not require the use of a PLL. Using the new C#-based simulation platform, I verified that the model is stable with noisy voltage measurements, using single-precision floating point variables, and using Euler's integration method for the solver, making the model suitable for microcontroller implementation. The simulation model was ported to C for implementation on the microcontroller used in the Mobile VISMA hardware (Infineon Tricore TC1796) and is used in the VISMA algorithm in this dissertation. The details of the mathematical model of the synchronous machine used in this algorithm are presented in the following section. This synchronous machine model is based on the synchronous machine model used in the SimPowerSystems toolbox of Matlab/Simulink and is thoroughly described in [21].

2.2 Mathematical Model of the Synchronous Machine

Figure 2.1 presents a simplified circuit representation of a wye-connected, two-pole synchronous machine. The synchronous machine comprises a stator and a rotor. In a two-pole machine, the stator has three windings geometrically (and electrically) displaced by 120°, whereas the rotor has a field winding, which is connected externally to a DC power source, and damper windings, which are not externally connected.

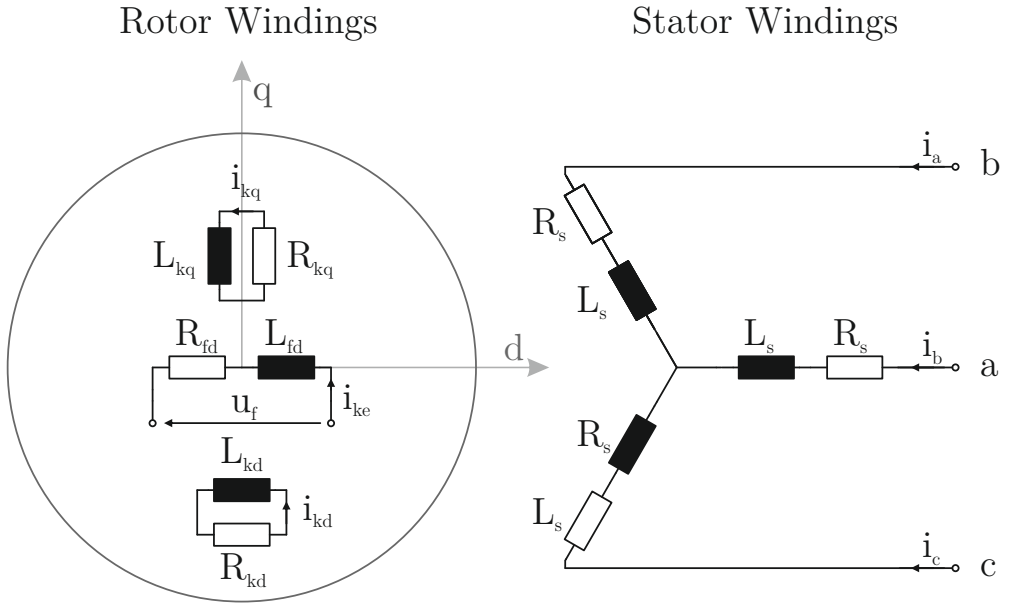


FIGURE 2.1: Circuit representation of a two-pole synchronous machine

Each of the three rotor windings is identical and can be modeled as a series connection of an inductor and resistor with an inductance L_s and resistance R_s, respectively. The field winding's magnetic axis is placed along the magnetic direct axis of the rotor and has an inductance and resistance, L_{fd} and R_{fd}, respectively. One of the damper windings' magnetic axes is along the direct axis of the rotor and has an inductance and resistance, L_{kd} and R_{kd}, respectively. The other damper winding's magnetic axis lay along the quadrature axis of the rotor and has an inductance and resistance, L_{kq} and R_{kq}, respectively.

The modeling of the synchronous machine can be done in the dq coordinate system, in which three-phase variables in the abc coordinate system are transformed to an equivalent two-phase coordinate system by means of the Park transformation [21].

Using this transformation, time-varying inductances are eliminated by referring the stator and rotor quantities to the rotating *dq* reference frame fixed to the rotor of the synchronous machine [21]. The angle ε is the angle between the direct axis of the *dq* coordinate system and the *a* axis of the *abc* coordinate system. Transformation from the *abc* coordinate system to the *dq* coordinate system, and from the *dq* coordinate system to the *abc* coordinate system is performed using the Park transformation (2.1) and inverse Park transformation (2.2), respectively.

$$\mathbf{P} = \begin{bmatrix} \frac{2}{3}\cos(\varepsilon) & \frac{2}{3}\cos(\varepsilon - \frac{2}{3}\pi) & \frac{2}{3}\cos(\varepsilon + \frac{2}{3}\pi) \\ -\frac{2}{3}\sin(\varepsilon) & -\frac{2}{3}\sin(\varepsilon - \frac{2}{3}\pi) & -\frac{2}{3}\sin(\varepsilon + \frac{2}{3}\pi) \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \tag{2.1}$$

$$\mathbf{P}^{-1} = \begin{bmatrix} \cos(\varepsilon) & -\sin(\varepsilon) & 1 \\ \cos(\varepsilon - \frac{2}{3}\pi) & -\sin(\varepsilon - \frac{2}{3}\pi) & 1 \\ \cos(\varepsilon + \frac{2}{3}\pi) & -\sin(\varepsilon + \frac{2}{3}\pi) & 1 \end{bmatrix} \tag{2.2}$$

An arbitrary variable, $[u_a\, u_b\, u_c]^T$ in the *abc* coordinate system can be transformed to the variable $[u_d\, u_q\, u_0]^T$ in the *dq* coordinate system with:

$$\begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix} = \mathbf{P} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \tag{2.3}$$

and vice versa with:

$$\begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix} = \mathbf{P}^{-1} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \tag{2.4}$$

To write down the differential equations of the synchronous machine, we can start with defining the machine's electrical and mechanical parameters:

- R_s – stator winding resistance
- L_s – stator winding inductance
- L_{md} – d-axis stator winding magnetizing inductance
- L_{mq} – q-axis stator winding magnetizing inductance
- R_{kd} – d-axis damper winding resistance
- R_{kq} – q-axis damper winding resistance
- R_{lkd} – d-axis damper winding leakage inductance

R_{lkq} – q-axis damper winding leakage inductance
R_{fd} – d-axis exciter winding resistance
L_{lfd} – d-axis exciter winding leakage inductance
F – friction coefficient
J – rotor inertia

The simulation of the machine can be done in the per-unit system. The nominal ratings of the synchronous machine are used as the base quantities in the per-unit conversion. The properties of the machine which are needed for the per-unit conversion are:

P_n – nominal power
U_n – nominal voltage
f_n – nominal frequency
n – number of pole pairs

Based on this we can calculate:

$I_n = P_n/U_n$ – nominal current
$X_n = U_n/I_n$ – nominal impedance
$\omega_n = 2\pi f_n$ – nominal angular frequency

The normalized parameters of the synchronous machine in per unit are:

$R_{sn} = R_s/X_n$ – normalized stator resistance
$X_l = \omega_n \cdot L_l/X_n$ – normalized stator reactance
$X_{md} = \omega_n \cdot L_{md}/X_n$ – normalized d-axis stator magnetizing reactance
$X_{mq} = \omega_n \cdot L_{mq}/X_n$ – normalized q-axis stator magnetizing reactance
$R_{fdn} = R_{fd}/X_n$ – normalized d-axis field winding resistance
$X_{lfd} = \omega_n \cdot L_{lfd}/X_n$ – normalized d-axis field winding reactance
$R_{kdn} = R_{kd}/X_n$ – normalized d-axis damper winding resistance
$X_{lkd} = \omega_n \cdot L_{lkd}/X_n$ – normalized d-axis damper winding reactance
$R_{kqn} = R_{kq}/X_n$ – normalized q-axis damper winding resistance
$X_{lkq} = \omega_n \cdot L_{lkq}/X_n$ – normalized q-axis damper winding reactance
$H = \left(\frac{\omega_n}{n}\right)^2 \frac{J}{2P_n}$ – inertia constant
$R = \left(\frac{\omega_n}{n}\right)^2 \frac{F}{P_n}$ – friction constant

With these parameters, we can write a set of non-linear differential equations describing the dynamic behavior of the synchronous machine, which consists of flux linkage (per second) equations and mechanical equations.

We start with the flux linkage equations. The differential equations describing the stator direct- and quadrature-axis flux linkages, ψ_d and ψ_q, respectively, are:

$$\frac{d}{dt}\psi_d = \omega_n \left(u_d + \omega\psi_q + R_{sn} i_d\right) \tag{2.5}$$

$$\frac{d}{dt}\psi_q = \omega_n \left(u_q + \omega\psi_d + R_{sn} i_q\right) \tag{2.6}$$

The differential equation describing field winding flux linkage, ψ_{fd}, is:

$$\frac{d}{dt}\psi_{fd} = \omega_n \left(u_e + \frac{R_{fd}}{X_{lfd}} \cdot (\psi_{md} - \psi_{fd})\right) \tag{2.7}$$

The differential equations for the damper windings' flux linkages, ψ_{kd} and ψ_{kq}, are:

$$\frac{d}{dt}\psi_{kd} = \omega_n \cdot \frac{R_{kd}}{X_{lkd}} \cdot (\psi_{md} - \psi_{kd}) \tag{2.8}$$

$$\frac{d}{dt}\psi_{kq} = \omega_n \cdot \frac{R_{kq}}{X_{lkq}} \cdot (\psi_{mq} - \psi_{kq}) \tag{2.9}$$

The mechanical differential equations are:

$$\frac{d}{dt}\omega = \frac{1}{2H}\left(T_m - T_e - R \cdot \omega\right) \tag{2.10}$$

$$\frac{d}{dt}\varepsilon = \omega_n \cdot \omega \tag{2.11}$$

where ω is the normalized angular frequency of the rotor, ε is the rotor angle, T_m is the mechanical torque acting on the rotor, T_e is the electrical torque produced by the synchronous machine, and R is the friction constant.

In the differential equations above,

$$\psi_{md} = X_{ad} \cdot \left(\frac{\psi_d}{X_l} + \frac{\psi_{fd}}{X_{lfd}} + \frac{\psi_{kd}}{X_{lkd}} \right) \tag{2.12}$$

$$\psi_{mq} = X_{aq} \cdot \left(\frac{\psi_q}{X_l} + \frac{\psi_{kq}}{X_{lkq}} \right) \tag{2.13}$$

are the direct- and quadrature-axis magnetizing flux linkages, respectively, where

$$X_{ad} = (X_{md}^{-1} + X_l^{-1} + X_{lfd}^{-1} + X_{lkd}^{-1})^{-1} \tag{2.14}$$

$$X_{aq} = (X_{mq}^{-1} + X_l^{-1} + X_{lkq}^{-1})^{-1} \tag{2.15}$$

are the direct- and quadrature-axis armature reaction reactances. The electrical toque produced by the synchronous machine is given by:

$$T_e = \psi_d \cdot i_q - \psi_q \cdot i_d \tag{2.16}$$

where

$$i_d = -\frac{1}{X_l} \cdot (\psi_d - \psi_{md}) \tag{2.17}$$

$$i_q = -\frac{1}{X_l} \cdot (\psi_q - \psi_{mq}) \tag{2.18}$$

are stator currents in *dq* coordinates. In this model, the zero components of the flux linkage and current were ignored. The equations describing the zero-component of the stator flux linkage ψ_0 and the zero-component of the stator current, i_0, are given below for completeness, but are not used in the VISMA algorithm.

$$\frac{d}{dt}\psi_0 = \omega_n \left(u_0 - \frac{R_s}{X_l} \cdot \psi_0 \right) \tag{2.19}$$

$$i_{0s} = -\frac{1}{X_l}\psi_0 \tag{2.20}$$

Equations 2.5 to 2.18 represent the mathematical model of the synchronous machine and are used in the VISMA algorithm. In the VISMA, the mathematical equations describing the synchronous machine are solved for the currents. The

inputs to equations are the transformed grid voltages u_d and u_q as well as the mechanical torque T_m. The state variables are the magnetic fluxes Ψ_d, Ψ_q, Ψ_{fd}, Ψ_{kd}, Ψ_{kq}, as well as the angular frequency ω and the rotor angle ε. The outputs of the equations are the transformed phase currents i_d and i_q. These currents are the output of the simulation and can be transformed back to the *abc* coordinate system using the inverse Park transformation.

2.3 Numerical Methods for the Solution of the VISMA Differential Equations

The explicit Euler method is a first-order method for solving differential equations. The implicit Euler finite difference equation is given by:

$$y_{n+1} = y_n + \Delta t f(t_{n+1}) \tag{2.21}$$

Although the Euler method for solving differential equations is not accurate, it is the simplest numerical method and requires the least computational effort.

Runge-Kutta methods are a family of single-point methods for solving differential equations which evaluate $\Delta y = (y_{n+1} - y_n)$ as the weighted sum of several $\Delta y_i (i = 1, 2, ...)$, where each y_i is evaluated as Δt multiplied by the derivative function $f(t, y)$, evaluated at some point in the range $t_n < t < t_{n+1}$ [22]. The fourth-order Runge-Kutta method is one of the most popular methods for the numerical solving of differential equations and is described by the equation:

$$y_{n+1} = y_n + \frac{1}{6}(\Delta y_1 + 2\,\Delta y + 2 + 2\,\Delta y_3 + \Delta y_4) \tag{2.22}$$

where

$$\Delta y_1 = \Delta t\, f(t_n, y_n) \tag{2.23}$$

$$\Delta y_2 = \Delta t\, f\left(t_n + \frac{\Delta t}{2}, y_n + \frac{\Delta y_1}{2}\right) \tag{2.24}$$

$$\Delta y_3 = \Delta t\, f\left(t_n + \frac{\Delta t}{2}, y_n + \frac{\Delta y_1}{2}\right) \tag{2.25}$$

$$\Delta y_4 = \Delta t\, f(t_n, y_n + y_3) \tag{2.26}$$

Generally, higher-order integration methods e.g. the fourth-order Rugne-Kutta method are known to offer an advantage in terms of error over the Euler method [22]. Simulations were performed to compare the VISMA response using the Euler and Runge-Kutta methods for a number of different scenarios. The simulations showed that using the machine model described in Section 2.2, the difference between the results of simulations preformed using the Euler and Runge-Kutta methods is negligible.

Figure 2.2 shows the normalized *dq* currents obtained from simulations using the Euler and fourth-order Runge-Kutta methods and a simulation time step of 0.1 ms for the following scenario. Initially, the virtual torque acting on the rotor and the virtual exciter voltage are set so that the stator currents are equal zero. At time $t = 0.2\,\mathrm{s}$, a torque acting on the rotor is increased by 0.1 p.u.. In the figure, the traces representing the currents calculated using the Euler and Runge-Kutta methods overlap, indicating that both methods produce the same results.

Figure 2.3 shows the normalized active power P and reactive power Q obtained from simulations using the Euler and fourth-order Runge-Kutta methods for the following scenario. Initially, the virtual torque and exciter voltage are set so that the synchronous machine produces positive active power ($P = 0.5\,\mathrm{p.u.}$, $Q = 0\,\mathrm{p.u.}$), i.e. it feeds active power into the grid. At time $t = 0.2\,\mathrm{s}$ the grid voltage drops to 90% of the nominal grid voltage ($U_g = 0.9\,U_n$). The full grid voltage is restored at time $t = 0.8\,\mathrm{s}$. When the voltage drop occurs, the synchronous machine responds with a surge of positive reactive power. When the full grid voltage is restored at $t = 0.8\,\mathrm{s}$, the synchronous machine responds with a surge of negative reactive power.

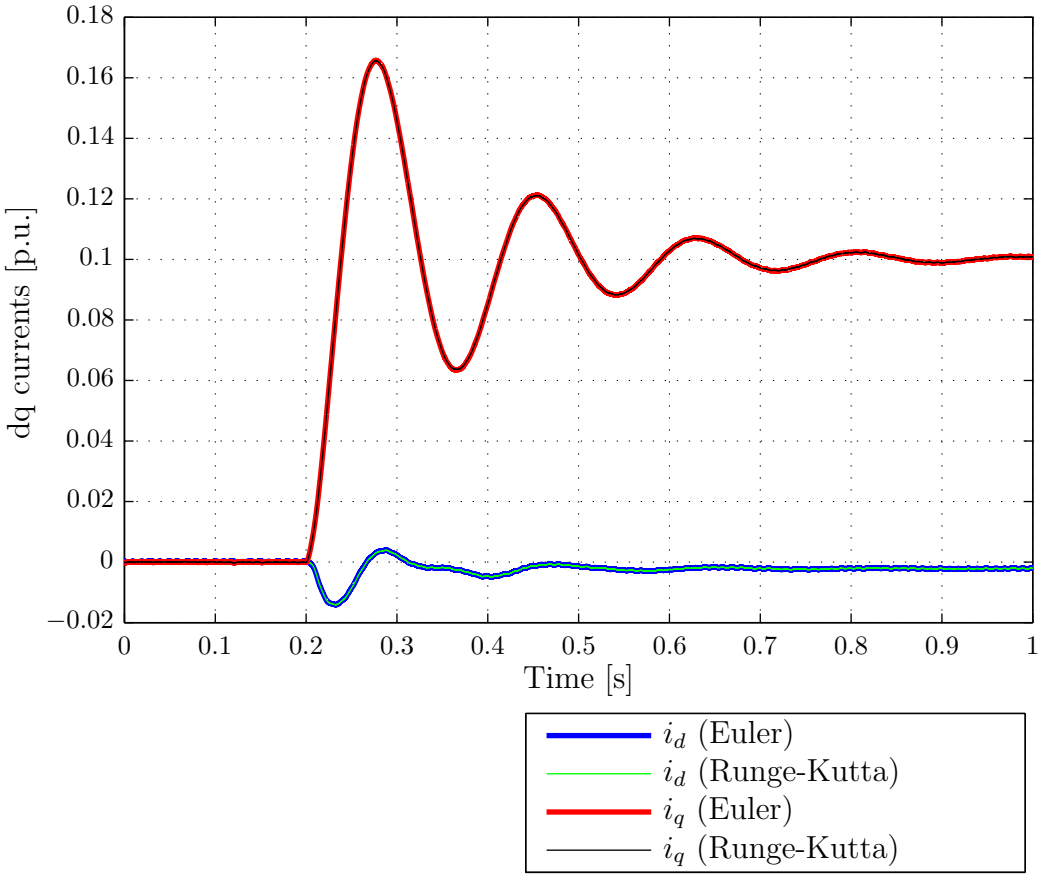


FIGURE 2.2: Simulation of the response of the synchronous machine to a step increase of the torque acting on the rotor using Euler and Runge-Kutta methods. Initially the stator currents are equal to zero when at time $t = 0.2\,\mathrm{s}$ the torque is increased by $0.1\,\mathrm{p.u.}$. The traces representing the currents calculated using the Euler and Runge-Kutta methods overlap, indicating that both methods produce the same results.

For this simulation scenario, the active and reactive powers calculated using the Euler and fourth-order Runge-Kutta methods overlap. Inasmuch, it can be concluded that the Euler implicit method is suitable for use in the VISMA algorithm, and because of its low computational requirements, it is used in the Mobile VISMA.

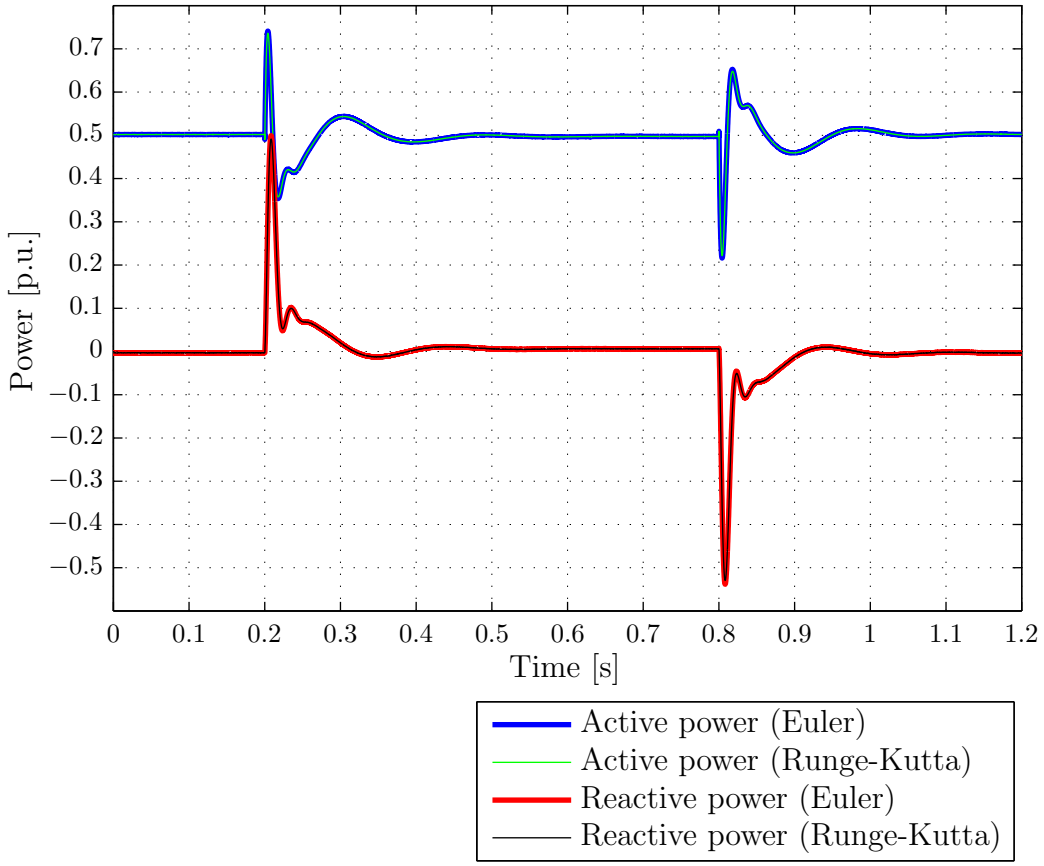


FIGURE 2.3: Simulation of the response of the synchronous machine to a sudden change of the grid voltage using Euler and Runge-Kutta methods. Initially the synchronous machine feeds active power into the grid ($P = 0.5\,\text{p.u.}$, $Q = 0\,\text{p.u.}$). At time $t = 0.2\,\text{s}$, the grid voltage drops to $U_g = 0.9\,U_n$. The full grid voltage is restored at time $t = 0.8\,\text{s}$. The traces representing the active and reactive power fed into the grid by the synchronous machine calculated using the Euler and Runge-Kutta methods overlap, indicating that both methods produce the same results.

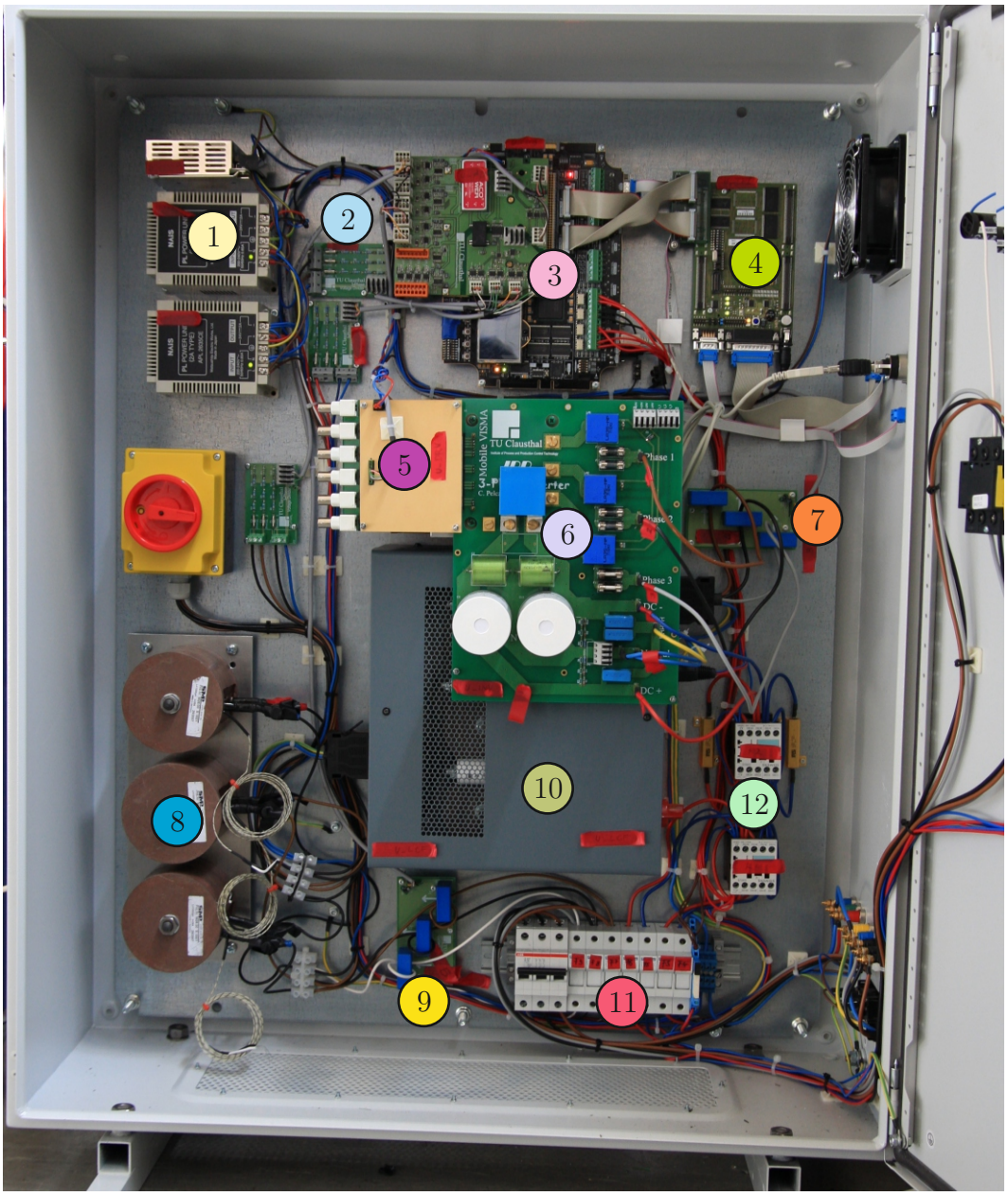
Chapter 3

Mobile VISMA Hardware

In this chapter the hardware designed for the Mobile VISMA is presented. The difference between the new Mobile VISMA hardware and the hardware used for previous VISMA versions described in [2], [3], and [19] is that, in the new hardware, analog signal processing has been reduced to a minimum, and the entire signal processing chain has been digitized. The VISMA synchronous machine simulation and current controller are implemented in a digital system using microcontroller and Field Programmable Gate Array (FPGA) technologies.

3.1 Experimental Hardware

The experimental hardware for the Mobile VISMA was designed with maximum configurational flexibility in mind. The complete hardware for the Mobile VISMA, excluding the batteries for the DC link, is enclosed in an electrical cabinet with the dimensions $800 \times 1000 \times 300$ mm and is shown in Figure 3.1. Although the volume of the cabinet is much larger than what would be feasible to install in a vehicle, the large cabinet size allows quick access to all the electrical components in the system and the possibility to expand the system with additional sensors and components in the development stage. The final vehicle-ready VISMA can be scaled down in size by removing redundant components and stacking the remaining components to fit a smaller enclosure. The Mobile VISMA hardware was designed to have a maximum current rating of 16 A Root Mean Square (RMS) and interface with the grid through a three-phase, 16 A connection. The maximum continuous power



1. DC power supply
2. Voltage dividers
3. FPGA motherboard with custom daughterboard
4. Microcontroller board
5. IGBT driver
6. Inverter board
7. Inverter-side current sensors
8. Grid-side filter inductors
9. Grid-side current sensors
10. Inverter-side LC filter box
11. Fuses
12. Precharging circuit for DC Link

FIGURE 3.1: Mobile VISMA cabinet (diagram Figure 3.3)

transfer between the grid and the VISMA is 11 kW. The complete experimental setup for the Mobile VISMA is described in Appendix A.

3.2 System Architecture

The hardware architecture of the Mobile VISMA prototype is presented in Figure 3.2. The system comprises sensors for voltage and current measurement, a data acquisition board which digitizes the analog sensor readings, and an FPGA motherboard [23], which hosts the Xilinx Spartan 3AN1400 FPGA [24], where the current control algorithms and algorithms related to data acquisition, signal processing, and supervisory control are implemented. Furthermore, the system comprises an Insulated Gate Bipolar Transistor (IGBT) driver board, an IGBT Intelligent Power Module (IPM), and power relays controlled from the FPGA, which are used to physically disconnect the inverter from the grid and from the DC link. The system also includes a microcontroller board [25], which communicates with the FPGA motherboard via a parallel bus with 16 data and 8 address lines.

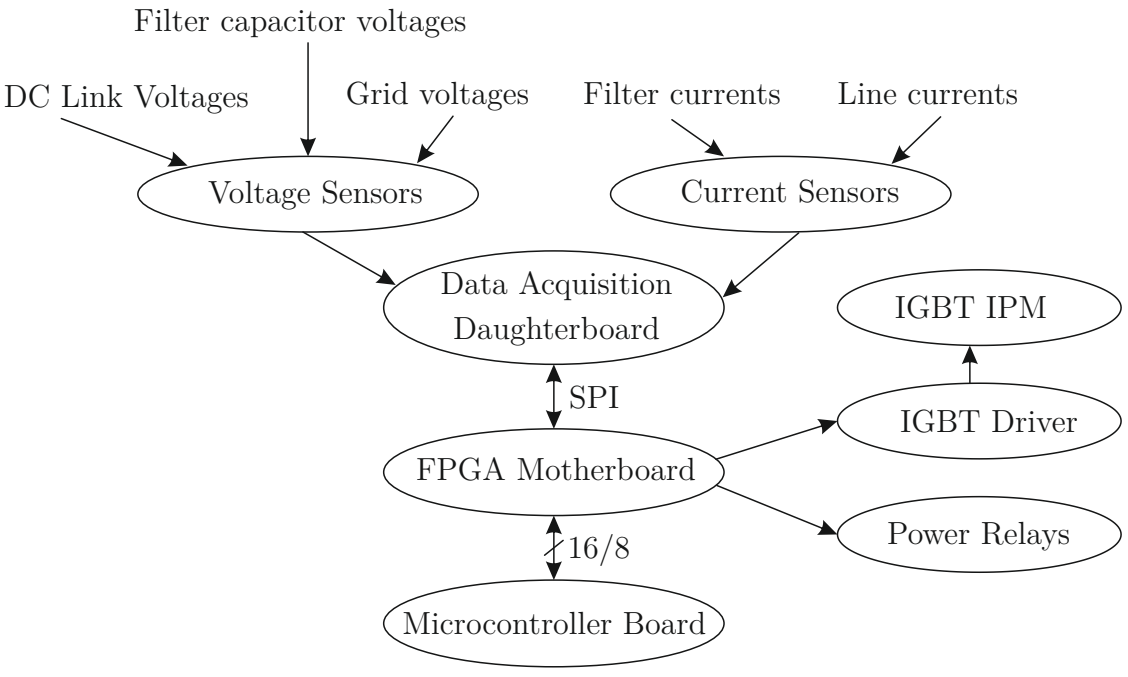


FIGURE 3.2: System architecture

Sensor readings are made by the FPGA and stored in the FPGA's internal memory. The FPGA is programmed to behave like a slave memory to the microcontroller, allowing the microcontroller to read measurements stored in the FPGA, set the desired current values for the current controller, and send other control data to the FPGA. The VISMA machine model simulation is executed on the microcontroller.

3.3 Data Acquisition

Figure 3.3 shows a simplified schematic of the VISMA system with emphasis on data acquisition and signal flow. The custom-designed data acquisition board, which is mounted as a daughterboard on the FPGA motherboard, allows the measurement of the following currents and voltages:

- DC link voltages $\mathrm{U_{DC+}}$ and $\mathrm{U_{DC-}}$
- Filter capacitor voltages $\mathrm{u_{fa}}$, $\mathrm{u_{fb}}$, and $\mathrm{u_{fc}}$
- Grid voltages u_{ga}, u_{gb}, and u_{gc}
- Filter currents $\mathrm{i_{fa}}$, $\mathrm{i_{fb}}$, and $\mathrm{i_{fc}}$
- Grid currents $\mathrm{i_{ga}}$, $\mathrm{i_{gb}}$, and $\mathrm{i_{gc}}$

The Analog-to-Digital Converters (ADCs) are read out through the FPGA, and the readings are made available to all logic circuits implemented in FPGA as well as programs running on the external microcontroller (MCU) board.

Not all signals which can be measured by the data acquisition system are necessary for implementing a current controller. They were installed for testing different control algorithms and analysis. In a commercial version, redundant sensors can be left out to save costs. The essential measured variables are the filter currents, grid voltages, and DC link voltages.

To allow the implementation of a hysteresis current controller, the filter currents need to be measured with a high sampling frequency because of their fast rate of change. To estimate the maximum rate of change of the filter current, we have to consider the inductance of $\mathrm{L_{fi}}$ and the maximum voltage drop across it, u_{Lfi}.

$$\frac{di_f}{dt} = \frac{u_{L_{fi}}}{L_{fi}} \tag{3.1}$$

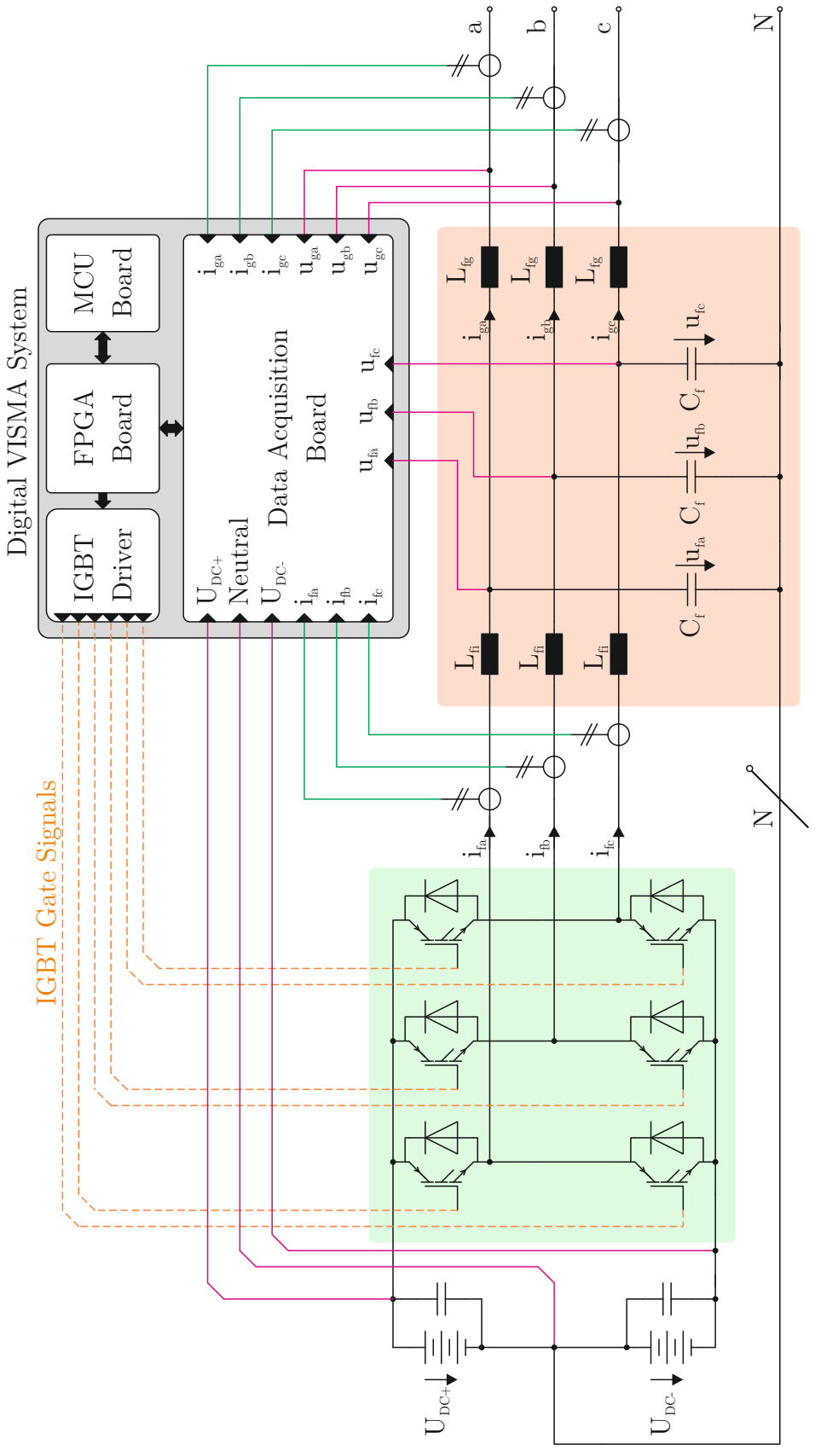


FIGURE 3.3: Simplified schematic diagram of the VISMA cabinet

The maximum voltage drop that can develop across the inductor L_{fi} is the difference between the positive DC link voltage and the negative grid voltage, and will be around 700 V, depending on the state of charge of the battery. If the inductance L_{fi} is known, using (3.1), the maximum rate of change of current can be calculated easily. For $L_{fi} = 3\,\text{mH}$ and $u_{L_{fi}} = 700\,\text{V}$, (3.1) becomes:

$$\frac{di_f}{dt} = \frac{u_{L_{fi}}}{L_{fi}} = \frac{700\,\text{V}}{3 \cdot 10^{-3}\,\text{H}} = 0.23\,\frac{\text{A}}{\mu\text{s}} \tag{3.2}$$

Only L_{fi} is considered under the assumption that high-frequency currents can flow into the filter capacitor, which represents the worst-case scenario (highest di/dt). Normally, the grid-side filter inductor L_{fg} and grid inductance will further limit the rate of change of the current.

To facilitate current measurement at a high sampling rate, closed-loop hall effect current transducers were used (LEM LA50), which can accurately follow currents with a rate of change of $50\,\text{A}/\mu\text{s}$ [26]. The transducer outputs are digitized with dual 14-bit ADCs (Analog Devices AD7367) [27]. Each current measurement channel has a separate ADC which allows simultaneous sampling of all channels and a maximum sampling rate of 1 MSPS per channel. Based on the calculations in (3.2), at this sampling rate, the current can change as much as 0.23 A within one sampling period. In the FPGA, for each phase a separate current controller is implemented. The controllers use the measured currents as feedback in the control loop and provide IGBT gate drive signals as outputs.

Voltage measurement in the system is implemented using voltage dividers connected to a 16-bit, multiplexed, 8-channel ADC with a maximum sampling rate of 250 kSPS (Analog Devices AD7689) [28]. The voltage measurement module is galvanically isolated from the remaining circuit using a digital isolator (Analog Devices ADum140x series) [29].

The ADCs of the data acquisition system are connected to the FPGA via Serial Peripheral Interfaces (SPIs). The voltage and current measurement channels are sampled continuously at their maximum sampling frequency by the FPGA. The measurement results are stored in the FPGA and are available to the controllers implemented in FPGA and to the microcontroller, which can access them via the parallel bus.

3.4 Line Filters

Figure 3.4 shows a single inverter phase connected to the grid through an LCL line filter. The filter comprises two inductors, the inverter-side inductor L_{fi} and the grid side inductor L_{fg}, which have internal resistances R_{fi} and R_{gi}, respectively. Furthermore, the filter comprises a capacitor C_f, which has an effective serial resistance R_c. In the figure, the grid is modeled as a series connection of a resistor R_g, inductor L_g, and AC voltage source U_{gen}.

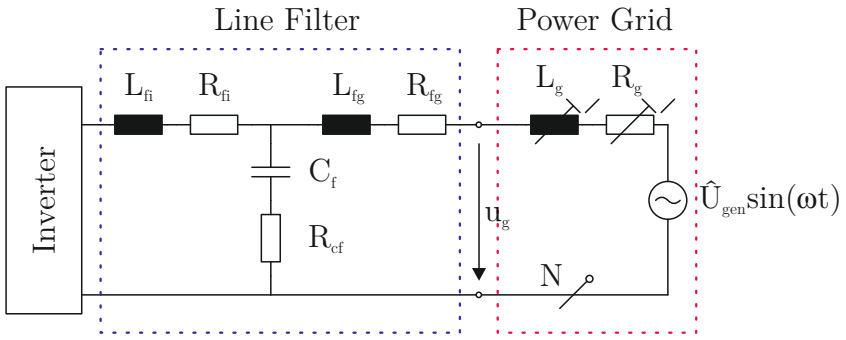


FIGURE 3.4: Single inverter phase connected to the power grid through an LCL line filter. The filter and grid form a resonant circuit, the resonant frequency of which depends on the filter as well as the grid impedance.

The LCL line filter and grid form an LCL resonant circuit. The parasitic resistance of the filter components as well as the resistance of the power lines introduce some damping in the system; however, care must be taken not to excite the system at its resonant frequency, as this may cause current and voltage ripple to exceed acceptable levels. Based on the derivations found in [30], the resonance frequency f_o of the system can be found:

$$f_o = \frac{1}{2\pi}\sqrt{\frac{L_{fg} + L_g + L_{fi}}{(L_{fg} + L_g)L_{fi}C_f}} \tag{3.3}$$

The resonance frequency f_o of the filter depends on the values of the filter components, which can be changed, as well as the grid impedance, over which we have no influence. The values of the passive components in the filter installed in the Mobile VISMA cabinet are presented in Table 3.1. In the experimental hardware, the grid-side filter inductor L_{fg} can be bypassed with a switch transforming the filter into an LC filter. Another switch can be used to toggle between two different filter capacitor values.

Symbol	Description	Value
L_{fi}	Inverter-side filter inductor	3 mH
L_{fg}	Grid-side filter inductor	1 mH or bypassed
C_f	Filter capacitor	selectable 3 μF or 15 μF

TABLE 3.1: Passive components used in the Mobile VISMA cabinet

In [31] we can find typical impedance values of local distribution network transformers and power lines. The reactance X_T of said transformers can range from 0.010 Ω for a 630 kVA transformer to 0.119 Ω for a 50 kVA transformer, corresponding to 0.032 mH and 0.379 mH, respectively, in a 50 Hz power network. The reactance of power lines depends on the type of conductor used and its length, where the reactance of uninsulated overhead lines is higher than that of underground cables and insulated overhead lines. The reactance X_L of power lines can range from 0.075 Ω/km for a 25 mm^2 underground cable to 0.358 Ω/km for an overhead line of the same cross-section, corresponding to 0.239 mH/km and 1.140 mH/km, respectively, in a 50Hz power network [31]. Based on these values, we can deduce that the grid inductance can vary from less than 0.1 mH in a strong grid to more than 1 mH in a weak grid.

Figure 3.5 plots the resonance frequency of the system consisting of the grid and filter as a function of grid inductance for different configurations of the LCL/LC filter. We can see that for an LC filter, the resonance frequency strongly depends on the grid inductance, and, if the grid inductance is small and the inverter switching frequency low, the resonance frequency may overlap with the switching frequency of the inverter, causing an excitation at the resonance frequency. With an LCL filter, the resonance frequency of the system changes little with changing grid impedance.

The inductors used in the VISMA cabinet are pot-core inductors, which have effective shielding and a low stray field [32]. These properties of pot-core inductors are much desired, as electromagnetic interference from the inductors can easily affect sensitive current and voltage measurement equipment in the cabinet. Also, this type of inductors can be placed in close proximity of one another without causing interference.

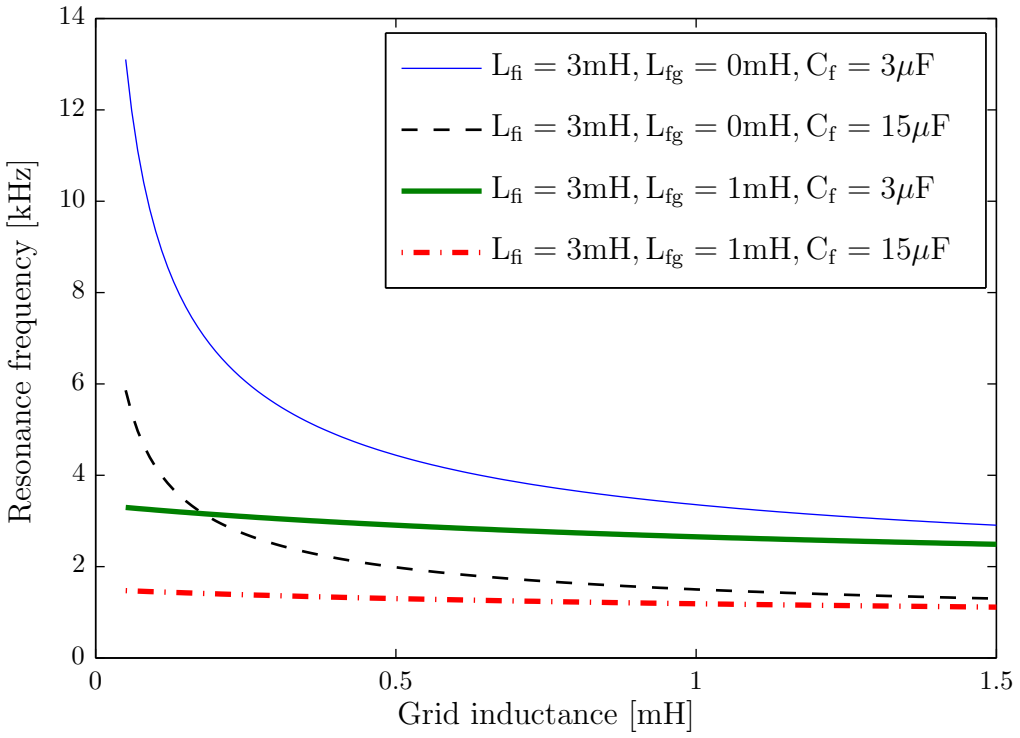


FIGURE 3.5: Resonance frequency of system consisting of the grid and LCL/LC filter as a function of grid inductance for different configurations of the LCL/LC filter

3.5 Inverter and Driver

The Mobile VISMA 3-phase inverter uses an IGBT-based IPM (Fuji 60MBP50-RA120 IGBT) for which a custom driver was designed. The IGBT is rated for a maximum collector-emitter voltage of 1200 V and a maximum collector current of 50 A. Unlike a normal IGBT, the IPM has integrated temperature protection provided by directly detecting the junction temperature of the IGBTs as well as pre-drivers which provide an amplifier for the driver, short circuit protection, overcurrent protection, and an undervoltage lockout circuit [33].

A block diagram of the IPM module with the custom-made IPM driver is shown in Figure 3.6. The driver uses an inverter interface and digital deadtime generator Integrated Circuit (IC) (Ixys IXDP630) to produce the gate drive signals. This IC takes single-phase inputs and expands them into two outputs to generate non-overlapping drive signals for the top and bottom IGBTs. The duration of the dead time can be controlled digitally by providing an external clock signal to the IC and is equal to 8 periods of this clock signal [34]. In many commercially available

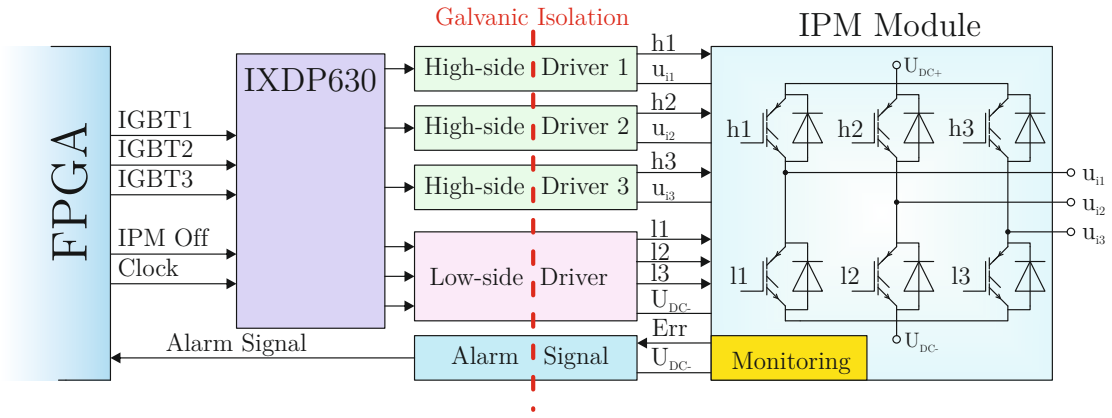


FIGURE 3.6: Block diagram of the IPM driver based on the Ixys IXDP630 inverter interface and deadtime generator. Galvanic isolation in the system is realized using optocouplers and isolated DC-DC converters.

drivers, the deadtime is set by an RC resonator and can be adjusted using trimmer resistors. Setting equal deadtimes for all IGBTs using these drivers is difficult, and the frequency of the RC resonator varies with temperature. With the custom-built driver, the deadtime duration can be precisely controlled by providing a clock signal from FPGA, and the deadtime can be easily changed in software. The possibility to vary the deadtime allows investigating the influence of deadtime duration on the current controller performance.

The high-side and low side drivers shown in Figure 3.6 introduce galvanic isolation between the IPM and the control electronics. The drivers use optocouplers and isolated DC-DC converters to realize the galvanic isolation. The output of the drivers are 15 V-level logic signals, which serve as inputs to the IPM's gate pre-drivers.

If any of the IPM's built-in protection systems detect abnormal operating conditions, such as an overcurrent, short-circuit, undervoltage of the power-source, or overheating, an alarm is released by the IPM [33], which can be used by the FPGA to shut down the inverter. The IPM driver also implements galvanic isolation in the alarm signal path.

3.6 Applications

The experimental Mobile VISMA hardware presented in this chapter does not have a compact design, but the system can be redesigned to fit a much smaller enclosure, allowing integration into a vehicle. In the current setup, the microcontroller board, FPGA motherboard, and data acquisition daughterboard are separate units. In a production version, these three boards could be integrated into a single unit to save space, costs, and improve Electromagnetic Compatibility (EMC). Such an integrated VISMA controller board could be used with different types of VISMA systems, also in stationary applications, e.g. for improving the power quality in the low-voltage network [35], for parallel operation with Uninterruptable Power Supply (UPS) systems [36], or for VISMA-enabled grid-tie inverters for distributed generators. Appendix B describes an FPGA board that we developed at the Institute of Process and Production Control Technology (IPP), which can be used as a base for future VISMA versions.

Chapter 4

Inverter Modeling and Hysteresis Controller Design

In this chapter, a simulation model of the inverter hardware with a hysteresis current controller is created. Experiments are performed in which the behavior of the simulated model is compared to the experimental results performed on the Mobile VISMA hardware, and the simulation model and parameters are optimized to make the simulations consistent with experimental results. The simulation model developed in this chapter will be later used for the development of new controllers, e.g. a PWM-based controller (see Chapter 5). Next, methods are discussed which can be used to quantitatively evaluate the performance of a current controller, and the performance of the hysteresis current controller is experimentally tested.

4.1 Inverter Model

Creation of a representative model of the inverter system is essential to optimize the controller design process. A good model can speed up design by allowing verification of the controller performance prior to implementation in hardware. In the Mobile VISMA, a separate current controller is used for each phase of the system; therefore, it is sufficient to create a model of a single leg of the inverter connected to the grid for simulation purposes.

Figure 4.1 shows a schematic diagram of a single phase of the inverter connected to the grid through an LCL filter. The LCL filter comprises an inverter-side

inductor L_{fi} with an internal resistance R_{fi}, a capacitor C_f with an Effective Serial Resistance (ESR) R_c, and a grid side inductor L_{fg} with an internal resistance R_{fg}. A single phase of the power grid is modeled as a series connection of a sinusoidal voltage source with an amplitude $\hat{U}_{gen}$, an inductor L_g, and a resistor R_g. The current controller's goal is to make the grid current i_g track the desired current i_d with the minimum possible error by controlling the switching states of the inverter's IGBTs.

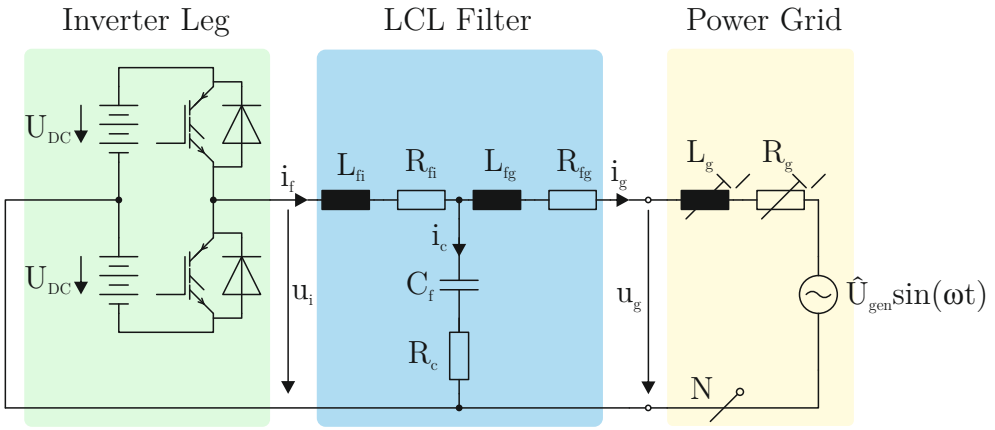


FIGURE 4.1: Single inverter phase connected to the power grid through an LCL line filter

In the operation of each inverter leg, we can distinguish three IGBT switching states:

(a) Top IGBT on

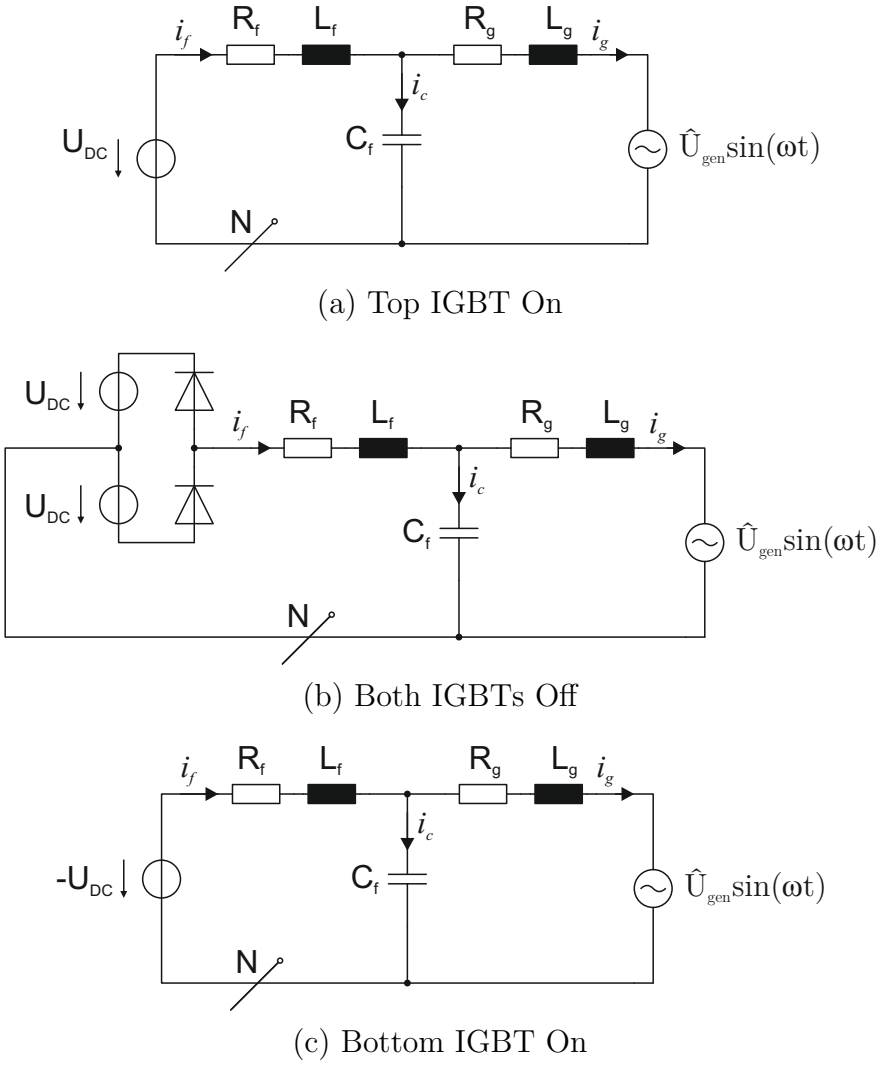
(b) Both IGBTs off

(c) Bottom IGBT on

Both IGBTs can never be on at the same time, as this would result in a short circuit and damage to the IGBT. The transition between the states is not instantaneous because of the switching times of the components. Between each transition from state (a), where the top IGBT is on, and state (c), where the bottom IGBT is on, and v.v., the inverter must spend some time in state (b), where both IGBTs are switched off. The time spent in state (b) is known as the deadtime and should be chosen based on the parameters and operating conditions of the IGBT.

Figure 4.2 shows simplified equivalent circuits of the inverter connected to the grid in the three possible switching states of the IGBTs. States (a) and (c) have nearly

identical equivalent circuits, except that the polarity of the DC voltage is reversed. In state (b) both IGBTs are switched off, but a current path for i_f through the IGBT's freewheeling diodes remains.



(a) Top IGBT On

(b) Both IGBTs Off

(c) Bottom IGBT On

FIGURE 4.2: Simplified equivalent circuits of inverter connected to the grid in different switching states

Because of the nonlinear, discontinuous nature of the system, a simulative approach to system analysis was chosen. The simulation software used was Piecewise Linear Electrical Circuit Simulation (PLECS) [37]. This software, made by Plexim GmbH, is available as a third-party toolbox for Matlab/Simulink and is designed for modeling and simulating power electronic systems.

Unlike the typical block diagrams used in Simulink, where the signal flow is unidirectional, PLECS allows the modeling of electrical systems using the more natural schematic representation. Based on the model, the software sets up the system

equations used in the simulation. PLECS makes use of the fact that if a physical model contains only linear and/or switching elements, it can be described by a set of piece-wise linear state space equations, and each state change of a switching element leads to a new set of space-state matrices describing the system [37].

4.2 Hysteresis Current Controller

The two-point hysteresis current controller is a well known controller which was used in all previous VISMA versions. Figure 4.3 shows a PLECS model of an ideal two-point hysteresis current controller feeding a current into the grid.

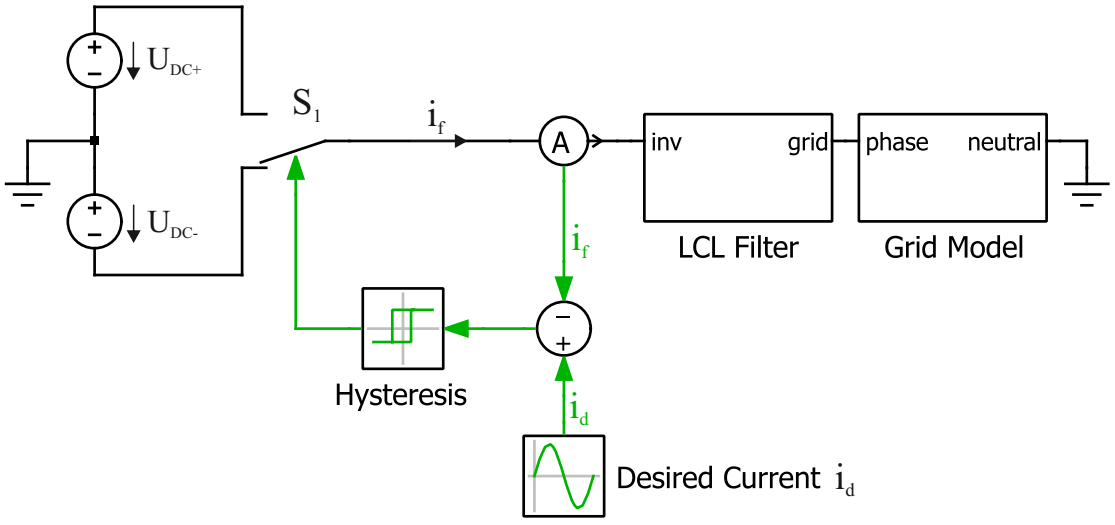


FIGURE 4.3: PLECS model of an ideal inverter with a two-point hysteresis current controller connected to the grid

The inverter leg is modeled as a switch which can toggle between the positive and negative DC terminals. The measured filter current i_f is compared to the desired current i_d. The control algorithm can be described as follows:

- if $i_d - i_f > I_{\delta-}$ then $S_1 \rightarrow DC+$
- if $i_d - i_f < -I_{\delta+}$ then $S_1 \rightarrow DC-$

where $I_{\delta+}$ and $I_{\delta-}$ are the positive and negative hysteresis limits, respectively.

There are two properties of the ideal hysteresis current controller which do not hold true for a real current controller. Firstly, in the ideal controller, switching

between the positive and negative DC-link terminals occurs instantaneously, which is not achievable using real components. Secondly, the ideal controller has no delay in the signal propagation path. The result is that the output current of the ideal hysteresis controller will, under normal operating conditions, remain within the hysteresis limits.

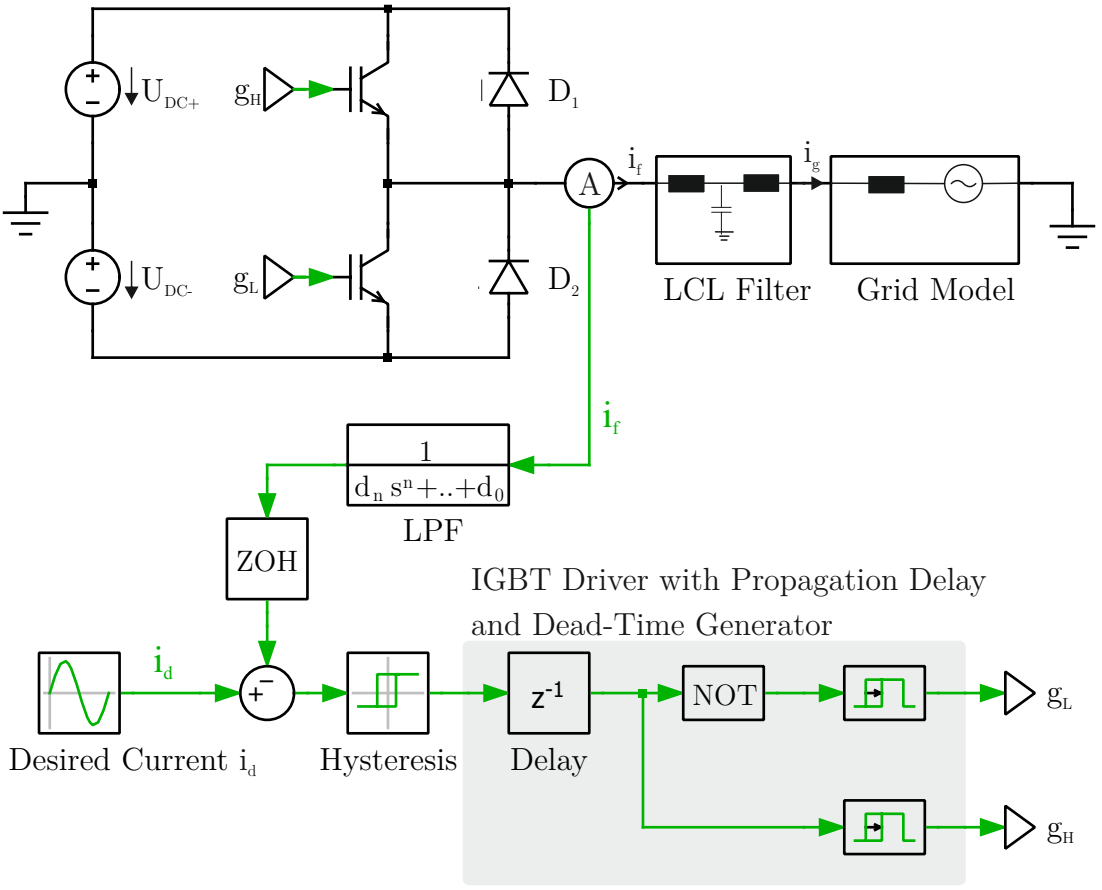


FIGURE 4.4: Realistic PLECS model of an inverter with a two-point hysteresis current controller connected to the grid. In the model, ADC sampling, deadtime, and the finite switching time of IGBTs are considered.

A more realistic PLECS model of the system is presented in Figure 4.4. In this model, the finite switching time of real components and delays in the signal propagation path are considered. The switches have been replaced by IGBTs with freewheeling diodes to model those in the IPM used in the Mobile VISMA hardware. The PLECS dynamic IGBT model with finite current slopes during turn-on and turn-off was used in the simulation model to account for the IGBT switching times. For the freewheeling diodes, a diode model which considers the reverse recovery effect was used [38]. The parameters for the IGBT and diode models

Parameter	Symbol	Value
Blocking voltage	V_{ces}	$1200\,\mathrm{V}$
Continuous collector current	I_c	$50\,\mathrm{A}$
Forward voltage	V_f	$1.3\,\mathrm{V}$
On resistance	R_{on}	$0.02\,\Omega$
Off resistance	R_{off}	∞
Rise time	t_r	$2 \cdot 10^{-6}\,\mathrm{s}$
Fall time	t_f	$3 \cdot 10^{-6}\,\mathrm{s}$
Stray inductance	L_{sig}	$18 \cdot 10^{-9}\,\mathrm{s}$
Initial current	i_0	$0\,\mathrm{A}$

TABLE 4.1: IGBT Simulation Parameters

Parameter	Symbol	Value
Forward voltage	V_f	$0.95\,\mathrm{V}$
On resistance	R_{on}	$0.0156\,\Omega$
Off resistance	R_{off}	∞
Continuous forward current	I_{f0}	$50\,\mathrm{A}$
Current slope at turn-off	$\frac{dI_r}{dt}$	$150 \cdot 10^{6}\,\mathrm{V}$
Reverse recovery time	t_{rr}	$200 \cdot 10^{-9}\,\mathrm{s}$
Peak recovery current	I_{rmm}	$15\,\mathrm{A}$
Probe inductance	L_{rr}	$1 \cdot 10^{-9}\,\mathrm{H}$

TABLE 4.2: Diode Simulation Parameters

were extracted from the IPM datasheet and are presented in Tables 4.1 and 4.2, respectively.

The IGBT driver was modeled using a delay element and turn-on delay elements. The delay element models the propagation delay of the gate drive signal, whereas the turn-on delay elements implement the deadtime generator. In the current measurement path, a Low-Pass Filter (LPF) transfer function represents the low-pass filtering effect of the sensor and the anti-aliasing filter. The LPF was implemented as a first-order lag element with a cutoff frequency $f_c = 400\,\mathrm{kHz}$ equal to the cutoff frequency of the anti-aliasing filter implemented on the data acquisition board. A Zero-Order Hold (ZOH) element represents ADC sampling.

The parasitic resistances of the passive components are included in the model. The inductors are modeled as a series connection of an ideal inductor and a resistor. Likewise, capacitors are modeled as a series connection of an ideal capacitor and a resistor.

4.2.1 Verification of the simulation model

Experiments were set up to compare the behavior of the PLECS model of the inverter and current controller to the hysteresis current controller implemented on the Mobile VISMA hardware. The outputs of the inverter were permanently short-circuited to the neutral line, as shown in Figure 4.5. A desired current with the form of a step function was fed into the short circuit. The measured resistance of the short-circuit path was $R_{ss} = 0.8\,\Omega$. The step function had an initial value of 0 A and a final value of 8 A. To verify that the parameter set used in the simulations is valid for different current values, the same experiment was repeated for different final values of the step function.

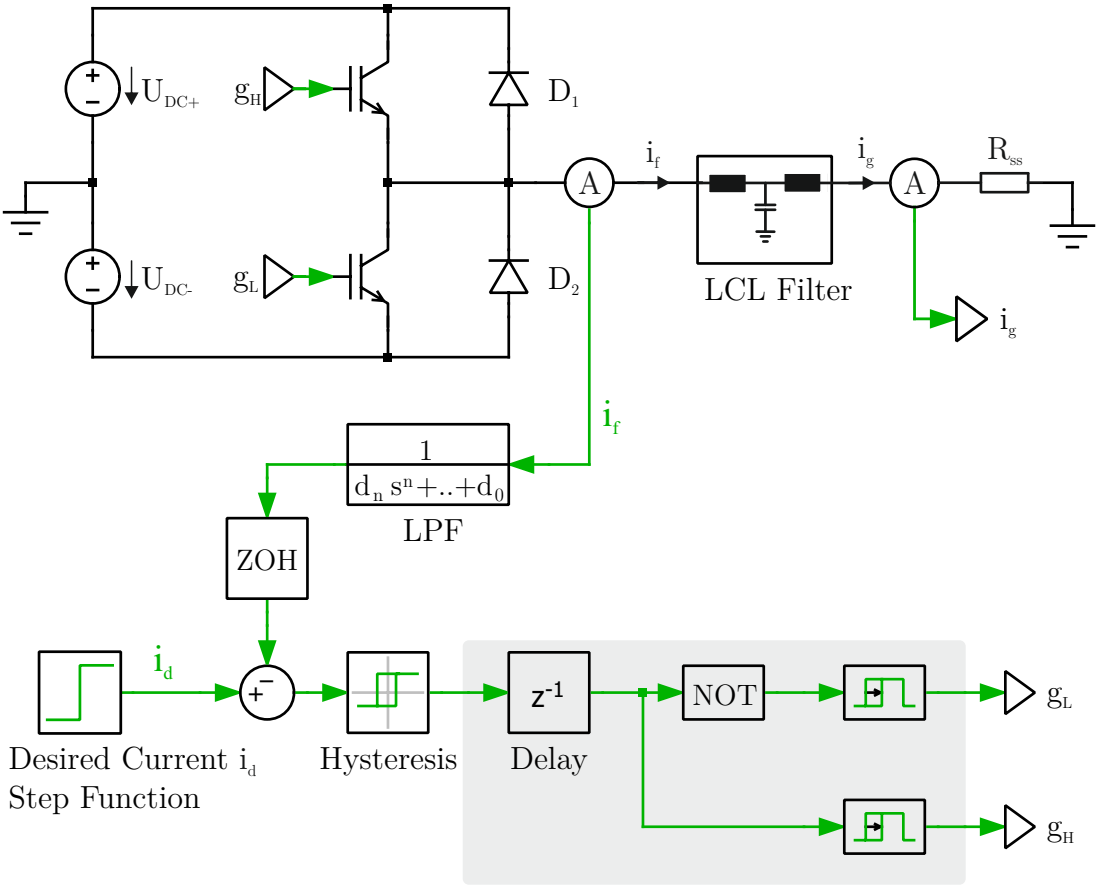


FIGURE 4.5: PLECS model of the inverter system with a hysteresis current controller used to find the step response of the system for comparison with experiments performed on the Mobile VISMA hardware

Simulations and experiments were performed for two configurations of the LCL filter. The datasheet values of the inductors were $L_{fi} = 3\,\text{mH}$ and $L_{fg} = 1\,\text{mH}$ in

both configurations. The capacitor values were $C_f = 3\,\mu\text{F}$ and $C_f = 15\,\mu\text{F}$ in the first and second configurations, respectively.

The results of the experiments and simulations were compared, and the parameters of the components in the simulation model were tuned to make the results consistent. Figures 4.6 and 4.7 show the step responses of the inverter running a hysteresis current control algorithm with $\pm 1\,\text{A}$ hysteresis limits obtained from the PLECS simulation with tuned parameters (TOP) and from measurements on the Mobile VISMA hardware (BOTTOM) for the two different configurations of the LCL filter. One can observe that the experimental and simulation results are similar. As a measure of similarity between the results, the following criteria can be used:

- IGBT switching frequency when $i_d = 0\,\text{A}$ and $i_d = 8\,\text{A}$
- Hysteresis limit violations when $i_d = 0\,\text{A}$ and $i_d = 8\,\text{A}$
- Resonance frequency f_0 of the LCL filter
- Damping of the grid current i_g

When the desired current i_d is set to $0\,\text{A}$, the measured and simulated IGBT switching frequencies differ, and are approx. $14\,\text{kHz}$ and $19\,\text{kHz}$, respectively, for the first LCL filter configuration. When $i_d = 8\,\text{A}$, both measured and simulated IGBT switching frequencies are similar, approx. $16\,\text{kHz}$. The reason is that the inductance of a physical inductor decreases with current flowing through it, and a higher inductance at low currents results in a lower switching frequency. Since in the simulation ideal inductors with current-invariant inductance are used, we can see a discrepancy in the IGBT switching frequencies for low currents.

The resonance frequency of the system was found by performing a Fast Fourier Transform (FFT) of the short-circuit current, i_g. Simulations and experiments yielded similar results. The resonance frequencies of the system with the first and second LCL filter configurations are $2.5\,\text{kHz}$ and $1.2\,\text{kHz}$, respectively.

Hysteresis violations in the simulations and experiments are of comparable magnitude. When $i_d = 0\,\text{A}$, both the upper and lower hysteresis limits are equally violated. When $i_d = 8\,\text{A}$, the violation of the lower hysteresis limit is higher, because during the deadtime, when both IGBTs are blocked, the current drops.

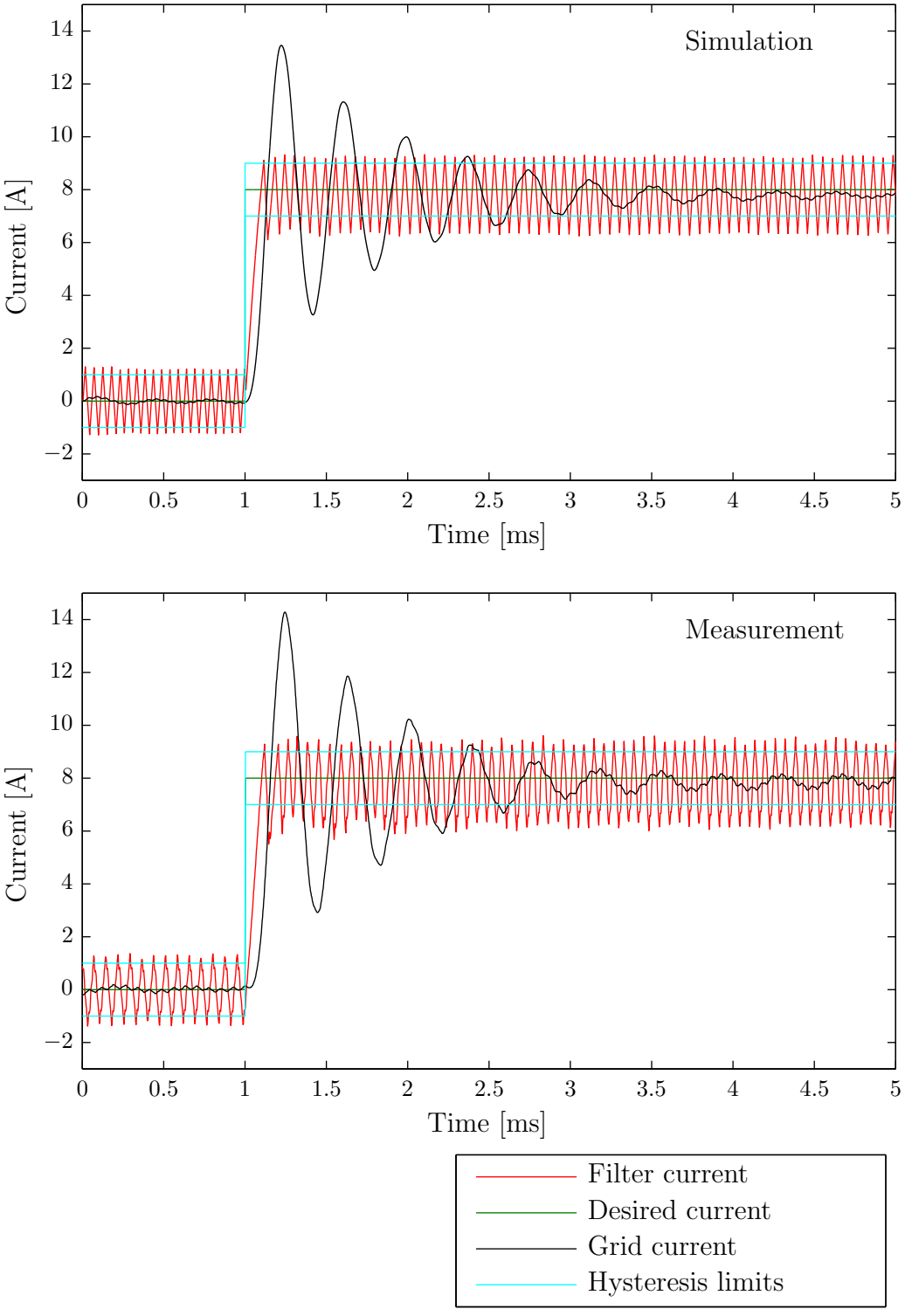


FIGURE 4.6: Step response of the hysteresis current controller obtained from simulation using a PLECS model of the Mobile VISMA inverter (TOP) and an experiment performed on the experimental hardware (BOTTOM). LCL filter configuration: $L_{fi} = 3\,\mathrm{mH}$, $L_{fg} = 1\,\mathrm{mH}$, $C_f = 3\,\mu\mathrm{F}$

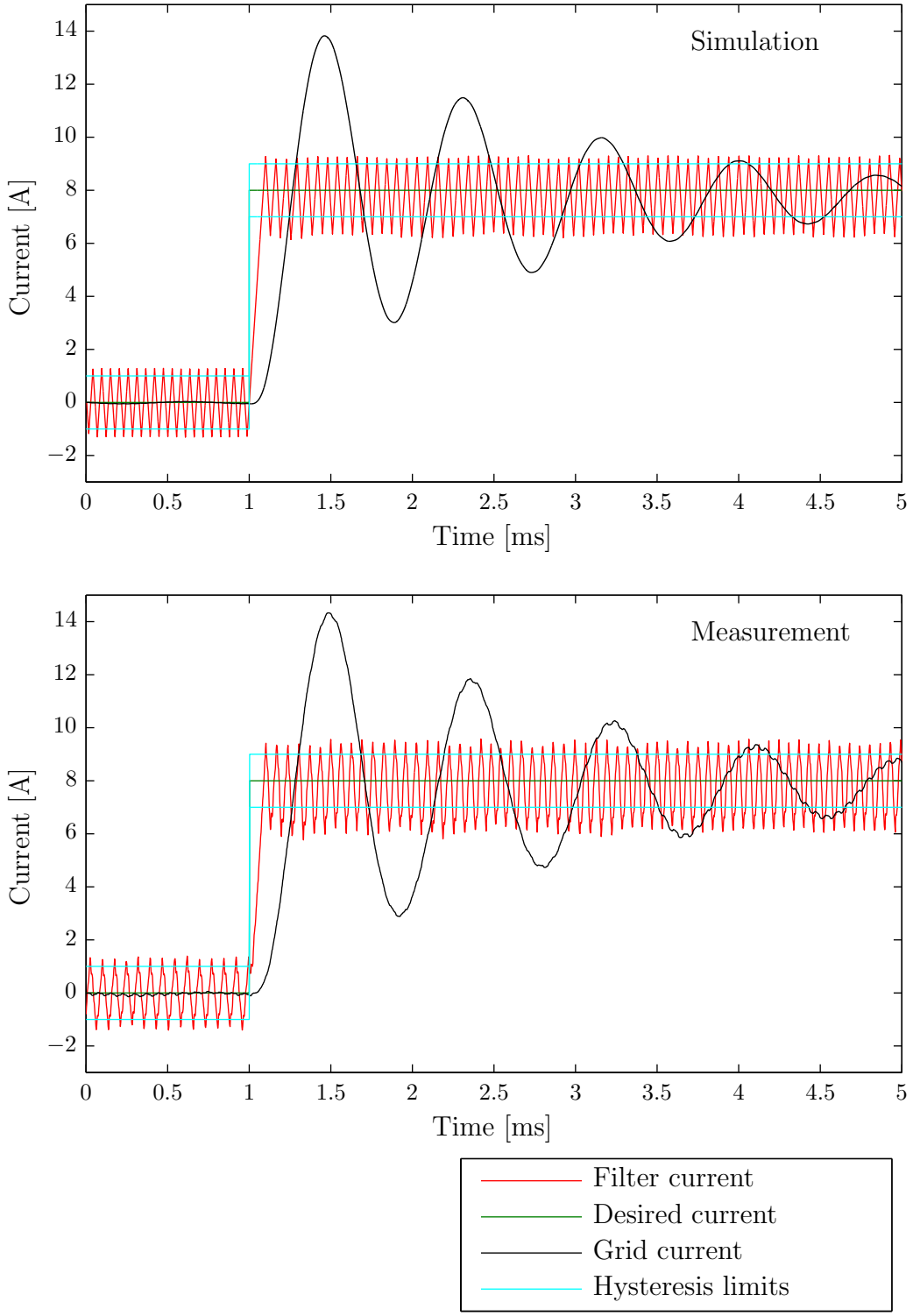


FIGURE 4.7: Step response of the hysteresis current controller obtained from simulation using a PLECS model of the Mobile VISMA inverter (TOP) and an experiment performed on the experimental hardware (BOTTOM), LCL filter configuration: $L_{fi} = 3\,\mathrm{mH}$, $L_{fg} = 1\,\mathrm{mH}$, $C_f = 15\,\mu\mathrm{F}$

Examining the current i_g in Figure 4.6 for the first filter configuration, we can see that oscillations in the current caused by the excitation with the step function decay at a similar rate and settle between the hysteresis limits after four oscillation periods in both simulation and experiment. This is also true for the current i_g in Figure 4.7 for the second filter configuration; however, since the resonance frequency of the second filter is lower, the actual settling time of the current for the second filter configuration is longer.

4.2.2 Tuning of simulation model parameters

Tuning of component parameters in the PLECS model had been done to obtain a simulation model behaving like the physical system. Because of the complexity of the system, several component parameters are often responsible for a single behavioral feature of the system, making it difficult to pinpoint which component parameters are physically responsible for a particular behavior.

The majority of the required changes in the simulation model were in the LCL filter model because of the non-ideal behavior of the passive components. The inductance values provided in the inductor manufacturer's datasheets delivered simulation results with higher IGBT switching frequencies and a higher resonance frequency than observed from experiment. The inductance values were increased until the simulation and experimental results were consistent. The inductor values used in the simulations were $L_{fi} = 4.2\,\mathrm{mH}$ and $L_{fg} = 1.2\,\mathrm{mH}$ for the filter and grid side inductors, respectively, in both tested filter configurations, whereas the inductances listed in the datasheets were $L_{fi} = 3\,\mathrm{mH}$ and $L_{fg} = 1\,\mathrm{mH}$, respectively. The parasitic resistances of the inductors were measured using a multimeter and found to be $R_{fi} = 0.2\,\Omega$ and $R_{fg} = 0.1\,\Omega$ for the filter and grid side inductors, respectively. The resistance of the short circuit connection was measured to be $R_{ss} = 0.8\,\Omega$. Using these values, the damping in the simulations was much smaller than in the physical system. The reason behind this this are the frequency dependent losses in the inductors and the ESR of the capacitor. Frequency dependent losses in inductors consist of losses in the core material, losses in the conductor from the skin effect, which results in a frequency-dependent change of the effective cross-section of the conductor, magnetic field losses of the neighboring windings, radiation losses, and losses from additional magnetic shielding [32]. Additional damping in the system was introduced by increasing the internal resistances of

the passive components used in the inverter model to account for the frequency dependent losses.

The only parameter which needed adjustment outside the LCL filter was the gate signal propagation delay element. A longer propagation delay was introduced, which increased the magnitude of hysteresis limit violations to match those measured in the experiments.

4.2.3 Asymmetrical hysteresis limit violations

Asymmetrical violations of hysteresis limits cause the average value of the filter current i_f in one switching period to differ from the average value of the desired current i_d, creating a tracking error. The asymmetry of the hysteresis limit violations is influenced by two factors, the value of the desired current and the instantaneous grid voltage. In the step response of the hysteresis current controller shown in Figure 4.6, it can be seen that the hysteresis limit violations are asymmetrical for non-zero currents. In each IGBT switching cycle, during the deadtime, both IGBTs are off, causing the current to drop. The result is that in one switching period, the average current i_f is smaller than the desired current i_d. This is an example of how the current affects the hysteresis violation asymmetry.

To understand how the grid voltage affects hysteresis violation asymmetry, let us consider an inverter feeding a zero current into the grid. The measured grid voltage and filter current for this scenario are presented in Figure 4.8. The output voltage of the inverter is u_i and the instantaneous grid voltage is u_g (see Figure 4.1). The voltage that develops across the LCL filter is $u_{LCL} = u_i - u_g$. The rate of change of the filter current increases with an increasing u_{LCL}. During one switching period, the inverter output voltage u_i toggles between the positive and negative DC-link voltage, U_{DC+} and U_{DC-}, respectively. In one of the inverter switching states u_{LCL} is larger, causing the hysteresis limit to be violated more in that direction.

In Figure 4.8 it can be seen that if the grid voltage is positive, the hysteresis violation is in the negative direction. When feeding active power into the grid (i_d in phase with u_g), the asymmetrical hysteresis violation will cause the grid current to be smaller than the desired current. When drawing power from the grid (i_d in counterphase to u_g), the grid current will be larger than the desired current.

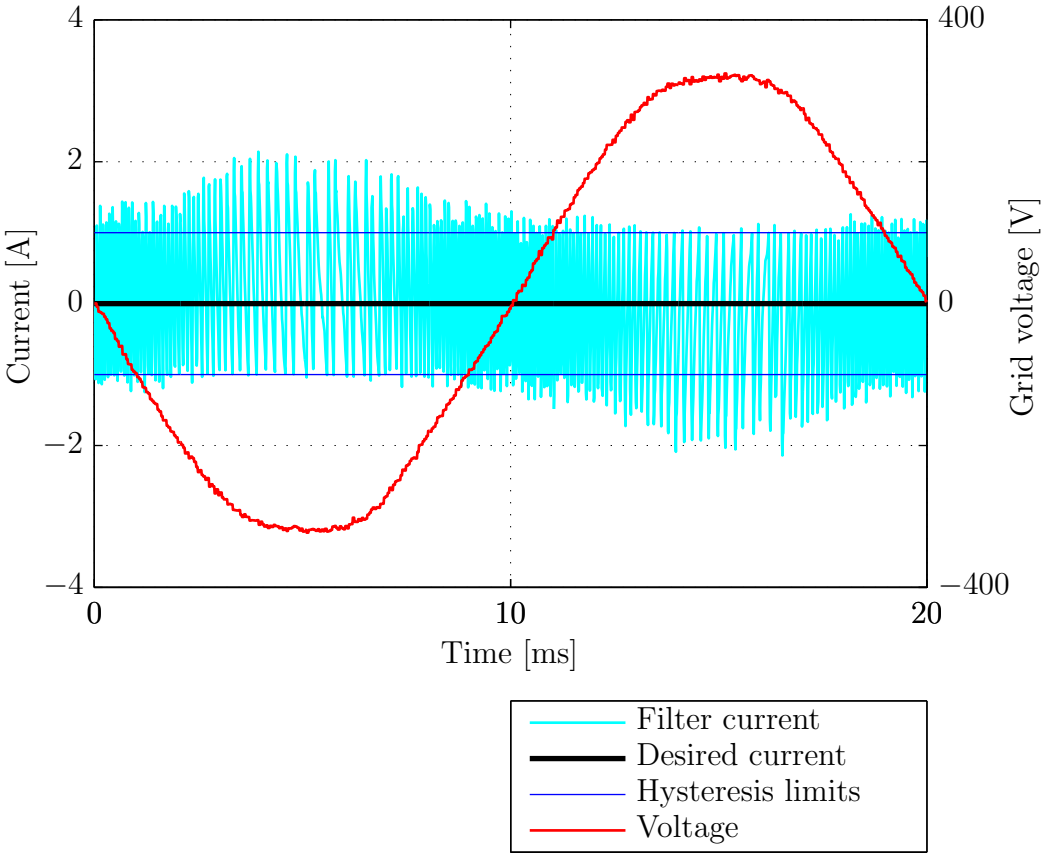


FIGURE 4.8: Measured filter current when desired current $i_d = 0\,\text{A}$ is fed into the grid. The grid voltage causes the hysteresis violation to be asymmetrical.

Hysteresis violations can be reduced by using faster inverter hardware, i.e. hardware with a higher ADC sampling frequency, less delay in the signal propagation path, and IGBTs with faster switching times that allow the reduction of the deadtime. In the Mobile VISMA hardware, the minimum IGBT deadtime is $4\,\mu\text{s}$, and it is the bottleneck in the system. After the current reaches a hysteresis limit, both IGBTs must stay off for the duration of the deadtime before any IGBT can be switched on [39]. During this time there is no control over the current. Newer generation IGBTs can be found with switching times below $1\,\mu\text{s}$ (e.g. 3rd and 4rd generation IGBTs described in [40] and [41]), which can significantly reduce the hysteresis limit violation problem, but can possibly cause EMC problems due to the higher du/dt.

4.3 Current Tracking Performance

The goal of a current controller is to feed in a desired current i_d into the grid. In [10] it is mentioned that a VISMA will only behave like a synchronous machine if the current tracking error is small. Therefore a controller is needed which can feed in the desired current without delay and keep the tracking error between the desired current i_d and the grid current i_g small. To compare different current controllers and hardware configurations, metrics are needed by which the current quality and tracking error can be assessed and compared.

4.3.1 Total harmonic distortion

One metric for evaluating the controller performance are the harmonic currents created by the system. According to the VDE-AR-N 4105 application guide [42], which describes the minimum technical requirements for the connection of generating facilities to the low-voltage network, the current harmonics and interharmonics generated by said facilities should comply with the following standards:

- DIN EN 61000-3-2 [43] with the limits for a class-A device for facilities with a nominal current $I_n \leq 16\,\mathrm{A}$ (see Appendix C.1)
- DIN EN 61000-3-12 [44], tables 2 and 3 for facilities with a nominal current $16\,\mathrm{A} < I_n \leq 75\,\mathrm{A}$ (see Appendix C.1)
- specified in VDE-AR-N 4105 for all other facilities

According to [42], harmonic currents are not attributed to the generating facility if they result from a distorted grid voltage or if the generating facility acts as a harmonic filter and through its operation continuously reduces the voltage harmonics.

The Mobile VISMA hardware is designed for a nominal current $I_n = 16\,\mathrm{A}$; therefore it will be treated as a class-A device under the EN 61000-3-2 standard. For class-A devices, EN 61000-3-2 [43] specifies absolute values of the individual harmonic limits up to the $40^{\,\mathrm{th}}$ harmonic; it does not specify a maximum limit for the Total Harmonic Distortion (THD).

The testing conditions requirements of the EN 61000-3-2 standard do not specify the impedance of the voltage source used in the conformity tests; it is only noted that the impedance should be small enough to meet the demands of the test. Although an inverter may meet the requirements set by the standard on the test grid, installed at another location with a different grid impedance, higher harmonic distortions are possible.

To analyze the harmonics of the currents fed into the grid by the current controller, a power analyzer (Fluke 434) [45] was used, which can measure current harmonics up to the 50^{th} harmonic on a single phase and calculate the THD. The THD percentage with respect to the 1^{st} harmonic is calculated based on the 2^{nd} to 40^{th} harmonics.

$$\text{THD}_{\%} = \frac{\sqrt{\sum_{n=2}^{40} {I_n}^2}}{I_1} \cdot 100\% \tag{4.1}$$

Although a limit for the maximum current THD is not specified in European standards, it is a good indicator of current quality for sinusoidal currents. Caution must however be taken when using this metric. Firstly, the THD is calculated for harmonics up to a specified harmonic number. It is possible for higher harmonics not included in the THD calculation to have a significant contribution to the current distortion. Secondly, the THD provides no information about the current tracking error. The grid current may be shifted in phase with respect to the desired current or have a different amplitude without affecting the THD.

The THD only informs us of how sinusoidal the signal is, so it only makes sense to use the THD metric if the desired current is sinusoidal. Since the desired currents produced by the VISMA machine model may contain some harmonics, the THD should not be used to judge the quality of VISMA currents.

4.3.2 Root mean square value of the current

For sinusoidal currents, alongside with THD, the RMS values of the desired and grid currents should be compared. The RMS value of the current over one period can be calculated as:

$$\text{RMS} = \sqrt{\frac{\sum_{k=0}^{n} i(k)^2}{n}} \tag{4.2}$$

where n is the number of measured samples per period. In the experiments, the RMS value of the grid currents was measured using an oscilloscope (Lecroy Wavejet 324A) [46] with a DC/AC current probe (Tektronix A622) [47].

4.3.3 Sum of square errors

Another metric for evaluating the current controller performance is the Sum of Square Errors (SSE) metric. The sum of square errors between the desired current i_d and the measured grid current i_g is calculated over a time period from $t = 0$ to $t = t_f$.

$$\text{SSE} = \sum_{t=0}^{t_f} (i_d - i_g)^2 \tag{4.3}$$

Because the SSE metric considers the difference between the desired and measured currents, it is a good indicator of current tracking performance. The lower the SSE, the better the tracking performance. Unlike the THD, the SSE can be used with both non-sinusoidal and sinusoidal currents.

In the Mobile VISMA a module was implemented in FPGA to calculate the SSE. The module calculates the average SSE over multiple periods of the current and outputs a unitless value indicative of the SSE which can be used for comparison purposes.

4.4 Transfer of Active Power using the Hysteresis Current Controller

In this section we shall consider the performance of the hysteresis current controller when the current fed into the grid is sinusoidal and in phase with the grid voltage, i.e. the inverter feeds active power into the grid, or counterphase to the voltage, i.e. the inverter draws active power from the grid.

4.4.1 Feeding power into the grid

Figure 4.9 shows the simulated (TOP) and measured (BOTTOM) grid voltage and inverter currents when feeding in a 16 A current into the grid using a system with the first LCL filter configuration ($L_{fi} = 3\,\text{mH}$, $L_{fg} = 1\,\text{mH}$, $C_f = 3\,\mu\text{F}$). Figure 4.10 shows results of the same experiment for the second filter configuration ($L_{fi} = 3\,\text{mH}$, $L_{fg} = 1\,\text{mH}$, $C_f = 15\,\mu\text{F}$).

As predicted by simulation, oscillations of the grid current occur, which are particularly large for the first filter configuration. The occurrence of these oscillations can be explained if we consider the range of IGBT switching frequencies.

Figure 4.11 shows the range of IGBT switching frequencies measured using the switching frequency analyzer implemented in FPGA for the first filter configuration. 0.1% of the switching frequencies lay below 2.5 kHz, and 10% of the switching frequencies lay between 2.5 kHz and 5 kHz. In Section 4.2.1 the resonance frequency of the system with the first LCL filter configuration was found to be approx. 2.5 kHz. Some IGBT switching frequencies are in the range of the resonance frequency of the system, exciting the resonance and creating oscillations in the grid current.

Figure 4.12 shows the range of IGBT switching frequencies for the second LCL filter configuration. The resonance frequency of this system calculated in Section 4.2.1 is approx. 1.2 kHz. The resonance frequency of the system and the IGBT switching frequencies do not overlap, which results in less ripple on the grid current, as visible in Figure 4.10.

To compare the quality of the currents fed into the grid for the two different LCL filter configurations, we can consider current harmonics (see Figure 4.13). For the first filter configuration the harmonic percentage of fundamental grows for higher harmonic numbers and peaks at the 49^{th} harmonic (2450 Hz), which corresponds to the resonance frequency of the system. For the second LCL filter configuration the harmonics are smaller, and there is a rise in the harmonics around the system's resonance frequency at the 23^{rd} harmonic (1150 Hz).

The red horizontal lines in Figure 4.13 represent the harmonic limits according to EN 61000-3-2, recalculated to percent of fundamental for a 16 A current. The harmonics limits specified by this standard are violated from the 23^{rd} to the 40^{th} harmonic for the first filter configuration. Harmonics above the 40^{th} harmonic are

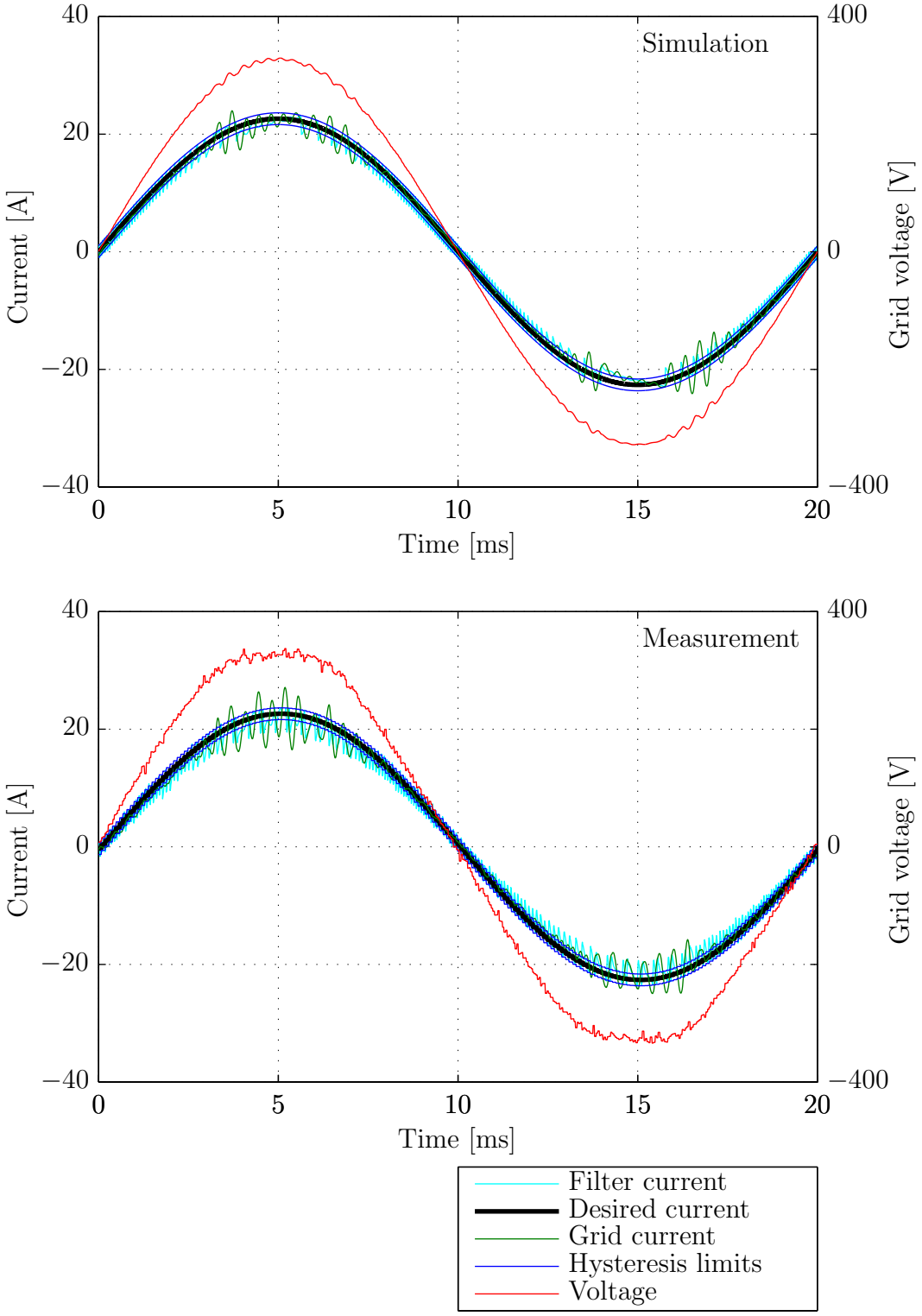


FIGURE 4.9: 16 A current fed into the grid using hysteresis current controller with ±1 A hysteresis limits. PLECS simulation (TOP) and experimental results (BOTTOM) are presented for an inverter with an LCL filter with the first configuration: $L_{fi} = 3\,\text{mH}$, $L_{fg} = 1\,\text{mH}$, $C_f = 3\,\mu\text{F}$

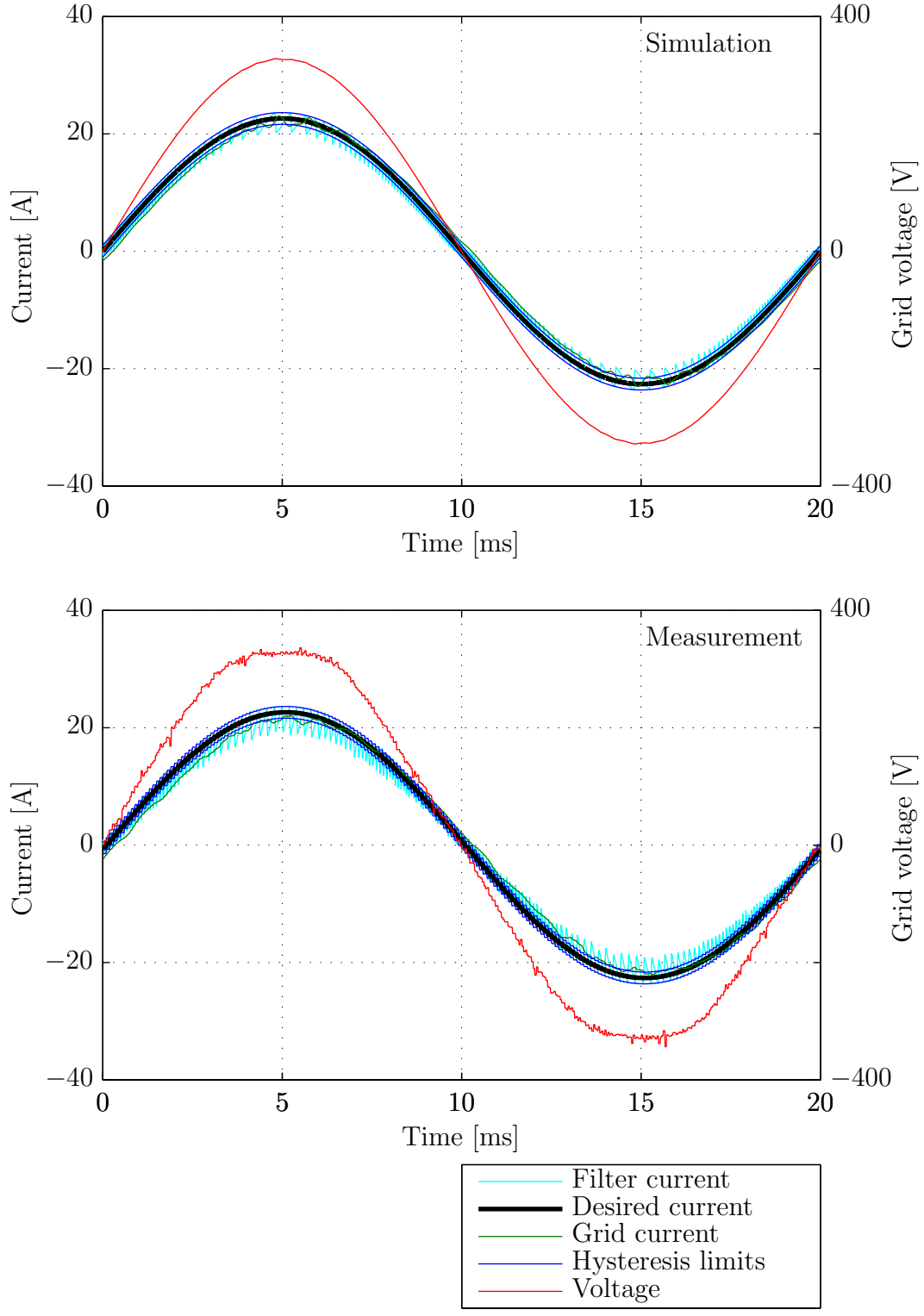


FIGURE 4.10: 16 A current fed into the grid using hysteresis current controller with ±1 A hysteresis limits. PLECS simulation (TOP) and experimental results (BOTTOM) are presented for an inverter with an LCL filter with the second configuration: $L_{fi} = 3\,\text{mH}$, $L_{fg} = 1\,\text{mH}$, $C_f = 15\,\mu\text{F}$

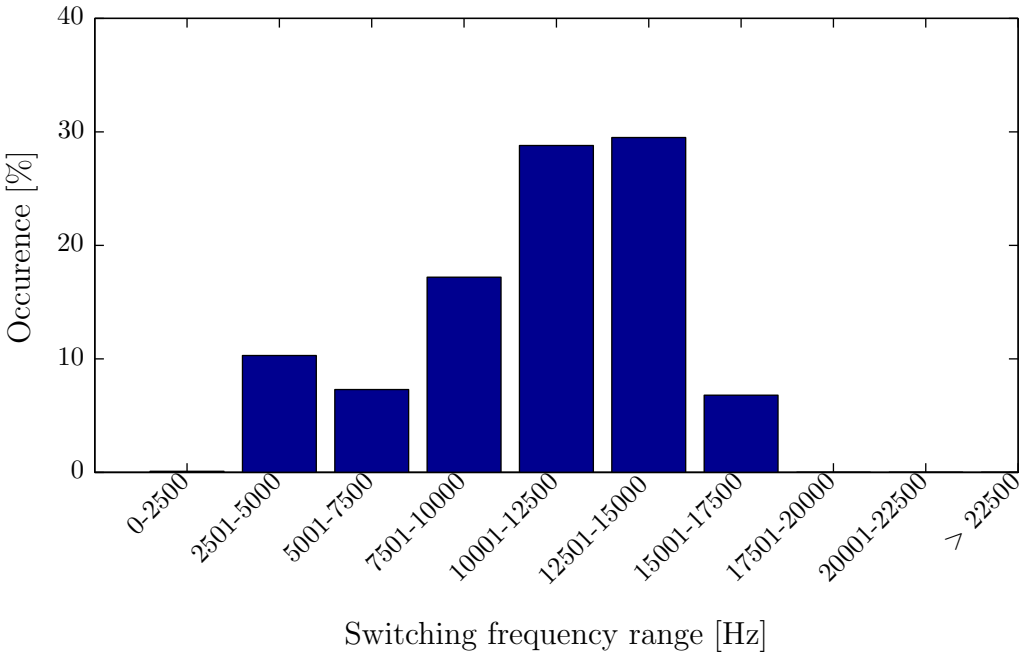


FIGURE 4.11: Switching frequency histogram for hysteresis controller feeding a 16 A current into the grid. LCL filter configuration: $L_{fi} = 3\,\text{mH}$, $L_{fg} = 1\,\text{mH}$, $C_f = 3\,\mu\text{F}$

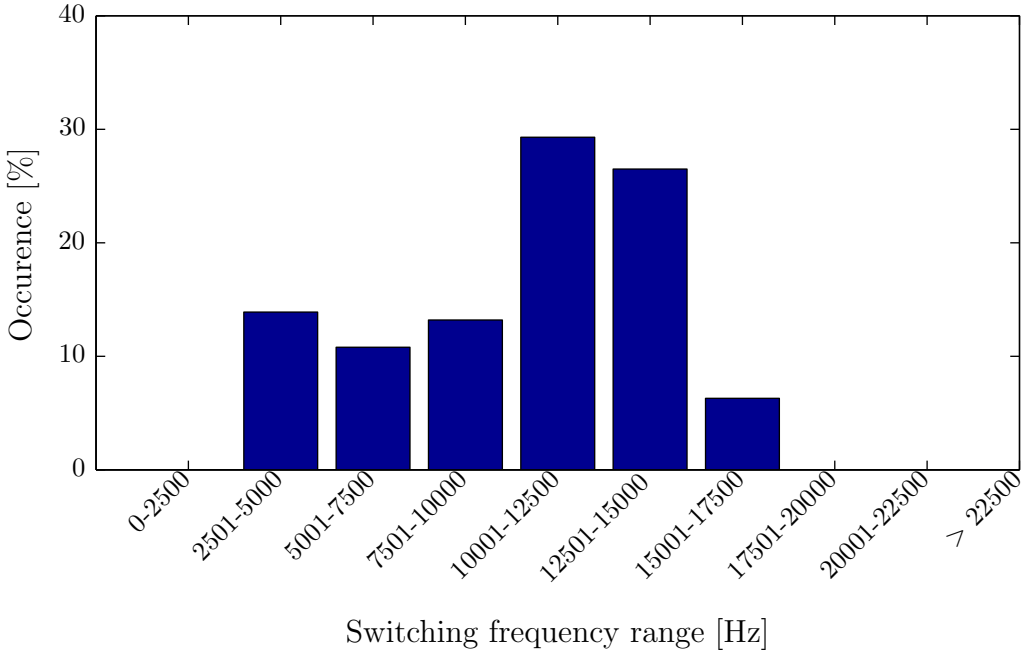


FIGURE 4.12: Switching frequency histogram for hysteresis controller feeding a 16 A current into the grid. LCL filter configuration: $L_{fi} = 3\,\text{mH}$, $L_{fg} = 1\,\text{mH}$, $C_f = 15\,\mu\text{F}$

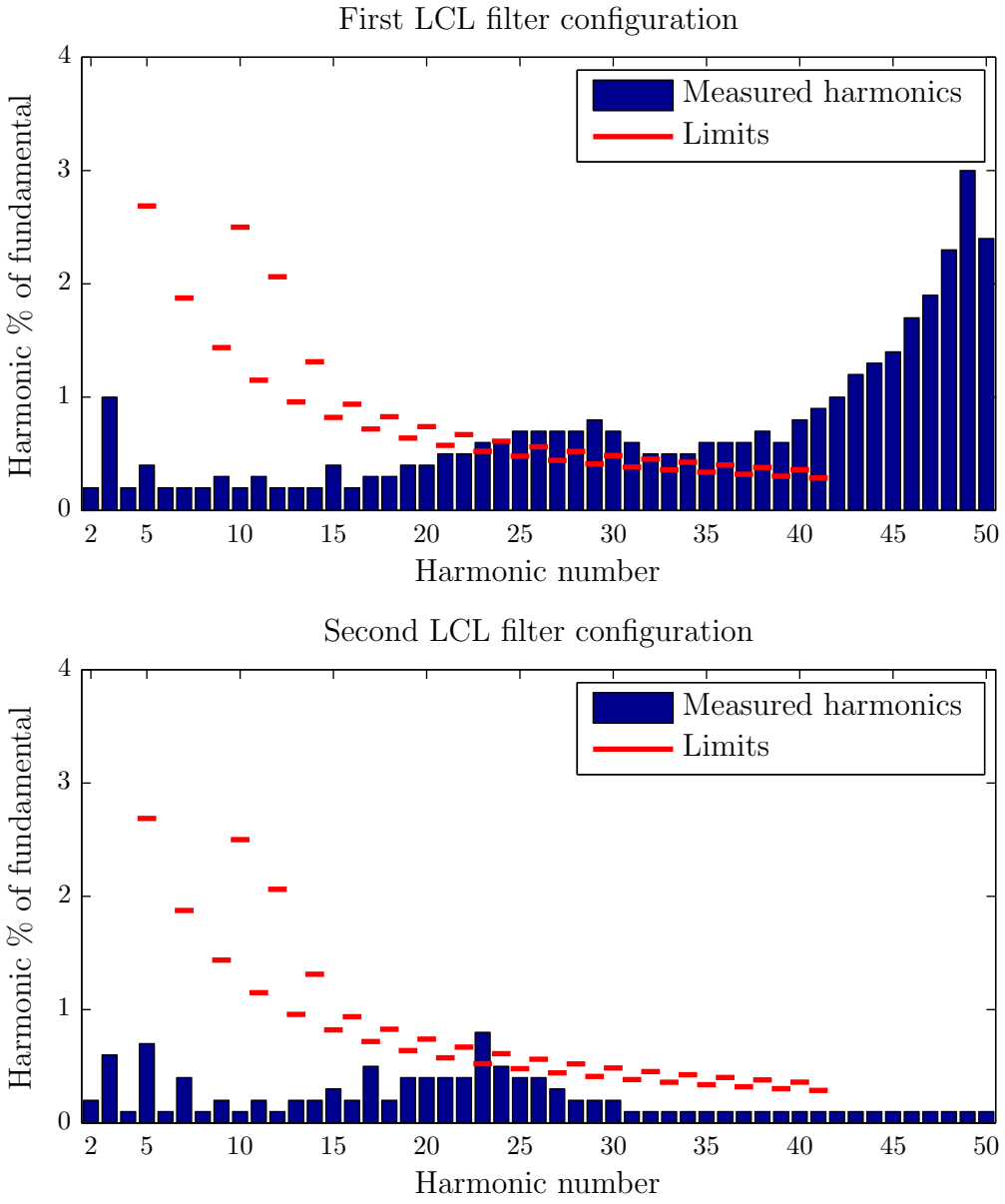


FIGURE 4.13: Harmonics of 16 A current fed into the grid using a hysteresis current controller with ±1 A hysteresis limits measured with a Fluke 434 power analyzer for the first (TOP) and second (BOTTOM) filter configurations. The red horizontal lines represent recalculated harmonic limits according to EN 61000-3-2.

Desired current	First filter configuration			Second filter configuration		
I_d [A]	I_g [A]	THD [%]	SSE	I_g [A]	THD [%]	SSE
1	0.9	13.5	744	1.4	16.7	722
2	1.9	12.0	1040	2.0	11.8	1039
3	2.9	8.5	1201	2.8	8.4	1234
4	3.8	6.6	1316	3.8	6.3	1358
5	4.8	5.4	1402	4.7	4.8	1498
6	5.8	4.9	1488	5.7	4.0	1588
7	6.8	4.4	1561	6.7	3.4	1688
8	7.8	4.0	1635	7.7	3.2	1784
9	8.9	3.7	1704	8.72	2.9	1845
10	9.9	3.4	1755	9.72	2.8	1914
11	10.8	3.1	1870	10.7	2.6	1982
12	11.7	2.9	1874	11.7	2.4	2036
13	12.7	2.7	1923	12.7	2.3	2080
14	13.8	2.6	1977	13.7	2.1	2141
15	14.8	2.6	2011	14.7	2.1	2207
16	15.8	2.4	2085	15.7	2.0	2263

TABLE 4.3: Feeding active power into the grid. RMS values, THDs, and tracking error SSE metrics of currents fed into the grid using a hysteresis current controller with $\pm 1\,\mathrm{A}$ hysteresis limits for two LCL filter configurations. First configuration: $L_{fi} = 3\,\mathrm{mH}$, $L_{fg} = 1\,\mathrm{mH}$, $C_f = 3\,\mu\mathrm{F}$. Second configuration: $L_{fi} = 3\,\mathrm{mH}$, $L_{fg} = 1\,\mathrm{mH}$, $C_f = 15\,\mu\mathrm{F}$

high, but the EN 61000-3-2 does not specify limits above the 40^{th} harmonic. For the second filter configuration the harmonic limits of EN 61000-3-2 are violated for the 23^{rd} harmonic, which corresponds to the resonance frequency of the system. In terms of harmonics, the second filter configuration, which has a lower cutoff frequency, performs better.

For a full evaluation of the current controller performance for both filter configurations, experiments were performed where sinusoidal currents of different amplitudes were fed into the grid using the hysteresis current controller with $\pm 1\,\mathrm{A}$ hysteresis limits. Table 4.3 summarizes the results of these experiments, showing the RMS values of the grid currents I_g, their THD, and the SSE values indicative of the tracking error. Because of hysteresis violations, the RMS value of the current fed into the grid is smaller than the desired current value. The second filter configuration leads to an overall lower THD. The SSE on the other hand is better for the first filter configuration, because the second filter configuration delays the current more, causing a larger phase shift between the desired and measured grid currents, which can, however, be compensated in the stationary case.

4.4.2 Drawing power from the grid

In the previous subsection, the performance of a hysteresis current controller feeding active power into the grid was considered. In this section, the same controller is used to draw active power from the grid to charge the batteries supplying the DC link. Figure 4.14 shows the simulated (TOP) and measured (BOTTOM) grid voltage and inverter currents when drawing a 16 A current from the grid for the first LCL filter configuration ($L_{fi} = 3\,\text{mH}$, $L_{fg} = 1\,\text{mH}$, $C_f = 3\,\mu\text{F}$). Figure 4.15 shows the results for the second filter configuration ($L_{fi} = 3\,\text{mH}$, $L_{fg} = 1\,\text{mH}$, $C_f = 15\,\mu\text{F}$). The distortion of the current while drawing power from the grid is smaller than when feeding power into the grid. The difference is especially evident for the first filter configuration, where oscillations of the current were conspicuous for the feed-in case (see Figure 4.9).

Figures 4.16 and 4.17 show the range of IGBT switching frequencies for the first and second filter configuration, respectively. When drawing power from the grid, the switching frequencies are higher and the switching frequency range is narrower (compare to Figures 4.11 and 4.12).

Figure 4.18 shows the current harmonics for the first and second filter configurations. The red horizontal lines in the figure represent the harmonic limits according to EN 61000-3-2, recalculated to percent of fundamental. Unlike when feeding power into the grid, when drawing power from the grid, the first filter configuration creates smaller harmonic currents, meeting the requirements set by the EN 61000-3-2 standard. For the second filter configuration, the limit for the 23^{rd} harmonic is violated.

Analogous to the feed-in case, experiments were performed where sinusoidal currents of different amplitudes were drawn from the grid using the hysteresis current controller with $\pm 1\,\text{A}$ hysteresis limits. Table 4.4 summarizes the results of these experiments, showing the RMS values of the grid currents (I_g), their THD, and the SSE values indicative of the tracking error.

When drawing power from the grid, the hysteresis violations cause the RMS value of the currents to be larger than the desired current values. The first filter configuration outperforms the second filter configuration both in terms of the THD and SSE.

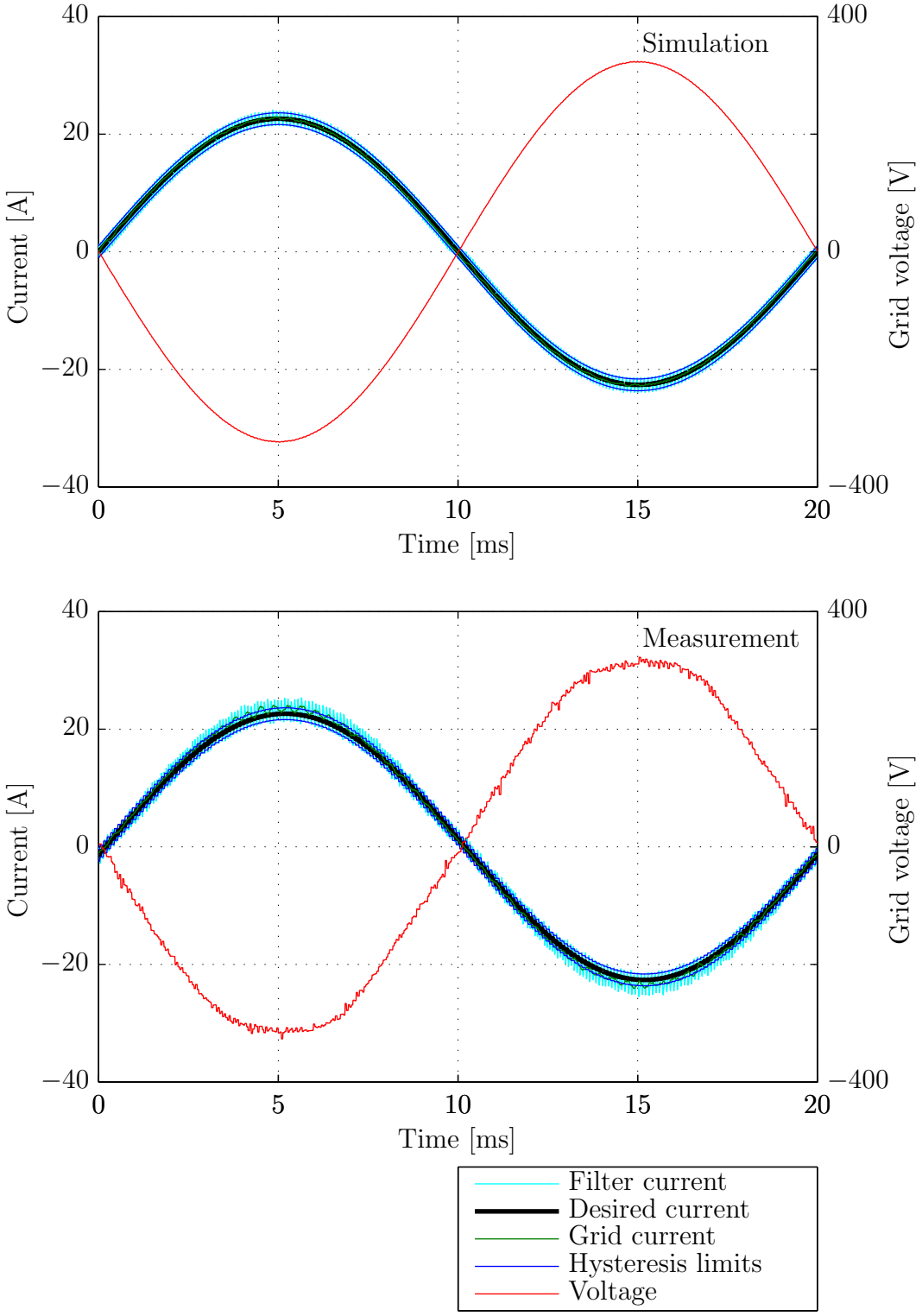


FIGURE 4.14: 16 A current drawn from the grid using hysteresis current controller with ±1 A hysteresis limits. PLECS simulation (TOP) and experimental results (BOTTOM) are presented for an inverter with an LCL filter with the first configuration: $L_{fi} = 3\,\text{mH}$, $L_{fg} = 1\,\text{mH}$, $C_f = 3\,\mu\text{F}$

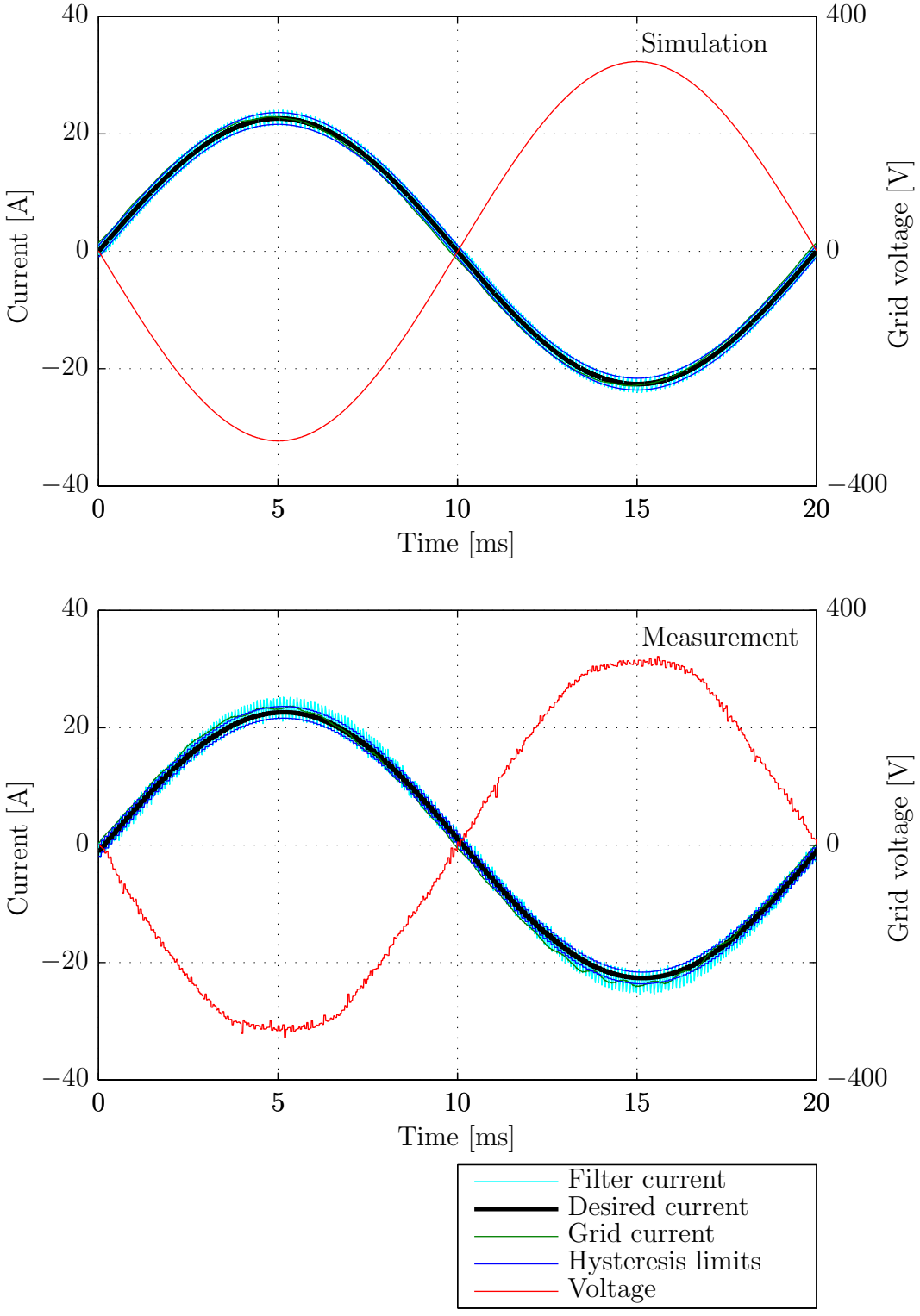


FIGURE 4.15: 16 A current drawn from the grid using hysteresis current controller with ±1 A hysteresis limits. PLECS simulation (TOP) and experimental results (BOTTOM) are presented for an inverter with an LCL filter with the second configuration: $L_{fi} = 3\,\text{mH}$, $L_{fg} = 1\,\text{mH}$, $C_f = 15\,\mu\text{F}$

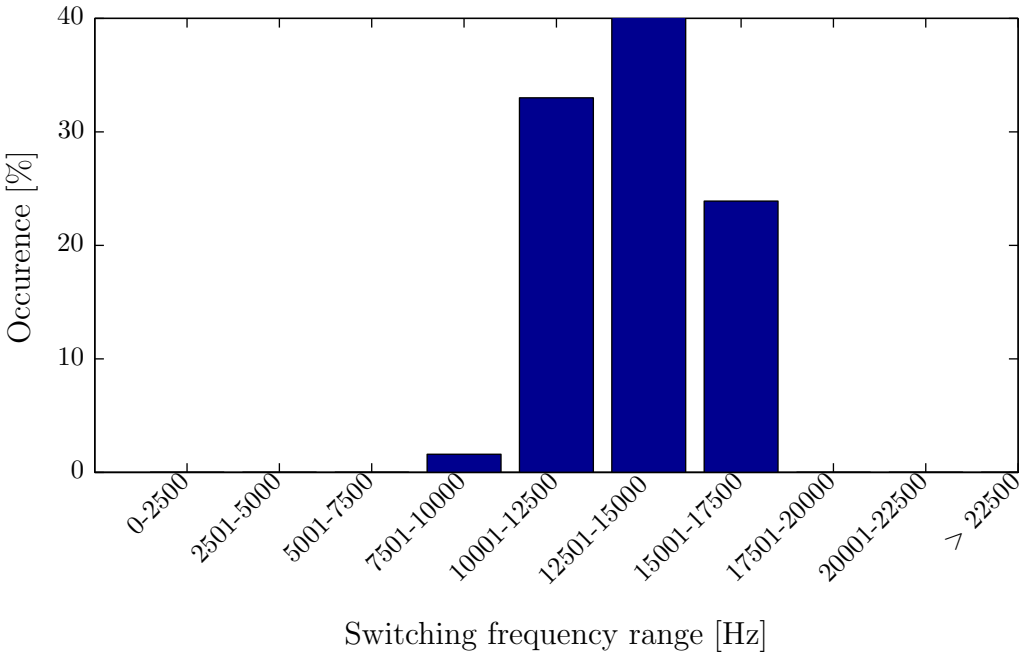


FIGURE 4.16: Switching frequency histogram for hysteresis controller drawing a 16 A current from the grid. LCL filter configuration: $L_{fi} = 3\,\text{mH}$, $L_{fg} = 1\,\text{mH}$, $C_f = 3\,\mu\text{F}$

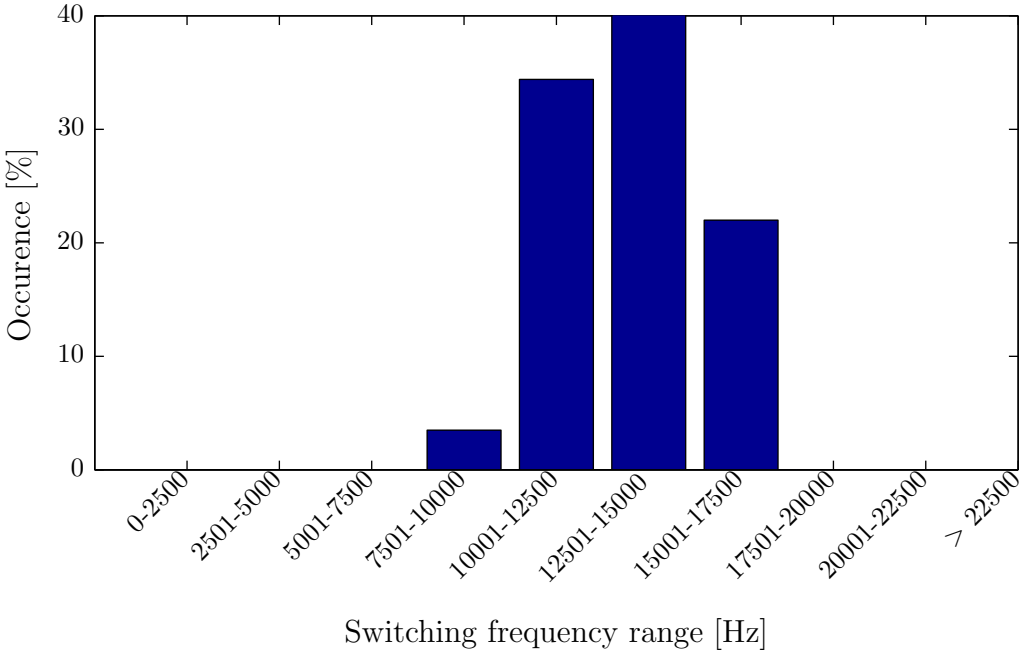


FIGURE 4.17: Switching frequency histogram for hysteresis controller drawing a 16 A current from the grid. LCL filter configuration: $L_{fi} = 3\,\text{mH}$, $L_{fg} = 1\,\text{mH}$, $C_f = 15\,\mu\text{F}$

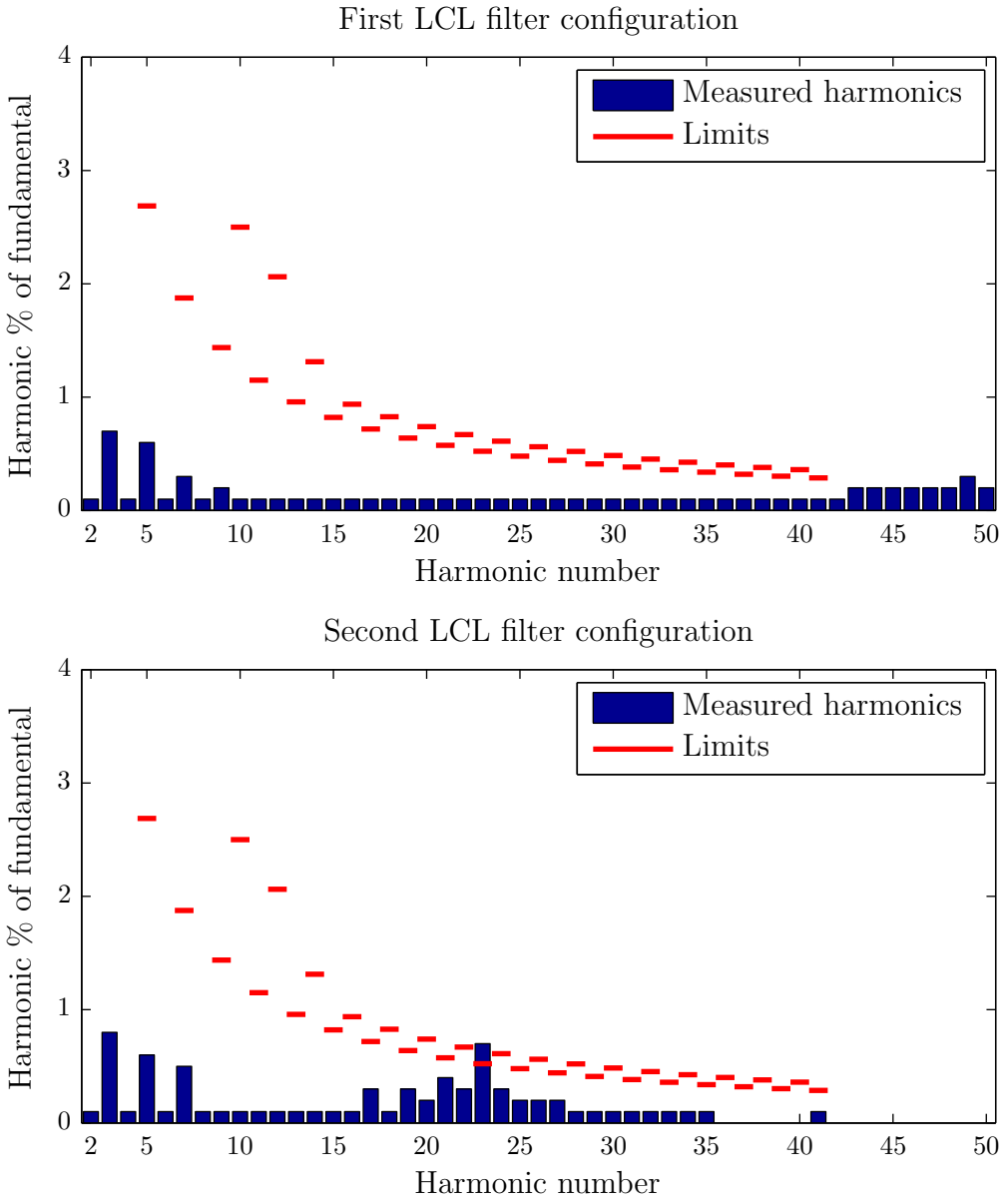


FIGURE 4.18: Harmonics of 16 A current drawn from the grid using a hysteresis current controller with ±1 A hysteresis limits measured with a Fluke 434 power analyzer for the first (TOP) and second (BOTTOM) filter configurations. The red horizontal lines represent recalculated harmonic limits according to EN 61000-3-2.

Desired current	First filter configuration			Second filter configuration		
I_d [A]	I_g [A]	THD [%]	SSE	I_g [A]	THD [%]	SSE
1	1.4	8.3	744	1.74	13.1	722
2	2.47	5.7	1040	2.49	9.0	1039
3	3.52	4.5	1201	3.64	6.5	1234
4	4.6	3.6	1316	4.39	5.5	1358
5	5.65	3.0	1402	5.16	4.6	1498
6	6.71	2.7	1488	6.77	4.0	1588
7	7.76	2.4	1561	7.82	3.5	1688
8	8.81	2.2	1635	8.84	3	1784
9	9.85	2.0	1704	9.89	2.7	1845
10	10.8	1.8	1755	10.9	2.5	1914
11	11.9	1.6	1810	11.9	2.2	1982
12	13.0	1.5	1874	12.9	2.0	2036
13	14.0	1.4	1923	13.9	1.9	2080
14	15.0	1.3	1977	15	1.9	2141
15	16.0	1.2	2011	16	1.7	2207
16	17.0	1.1	2085	17	1.7	2263

TABLE 4.4: Drawing active power from the grid. RMS values, THDs, and tracking error SSE metrics of currents drawn from the grid using a hysteresis current controller with ± 1 A hysteresis limits for two LCL filter configurations. First configuration: $L_{fi} = 3\,\text{mH}$, $L_{fg} = 1\,\text{mH}$, $C_f = 3\,\mu\text{F}$. Second configuration: $L_{fi} = 3\,\text{mH}$, $L_{fg} = 1\,\text{mH}$, $C_f = 15\,\mu\text{F}$

Chapter 5

Pulse Width Modulation Controller

As an alternative to the hysteresis current controller, which is characterized by a wide range of IGBT switching frequencies, a Pulse Width Modulation (PWM) controller with a fixed switching frequency can be used. In this chapter a PWM controller architecture is presented which can be used for current control in the VISMA system. A controller is designed based on this architecture with the aid of the simulation program PLECS. Finally, the controller is implemented in hardware and tested.

5.1 Controller Architecture

The basic architecture of the implemented PWM controller is presented in Figure 5.1. In the figure, the block *PWM Inverter* represents an inverter with a PWM modulator which operates with a fixed switching frequency. The inverter takes as input the desired inverter output voltage u_d and outputs a voltage u_i. The output of the inverter is connected to the grid through an LCL filter. The grid voltage u_g and filter current i_f are measured and used in the control loop.

In this architecture, there is one current feedback controller and two feed-forward controllers [48]. The feedback controller, G_C, can be a Proportional Integral (PI) controller with the transfer function $G_c(s) = K_p + K_i/s$. It uses the error current

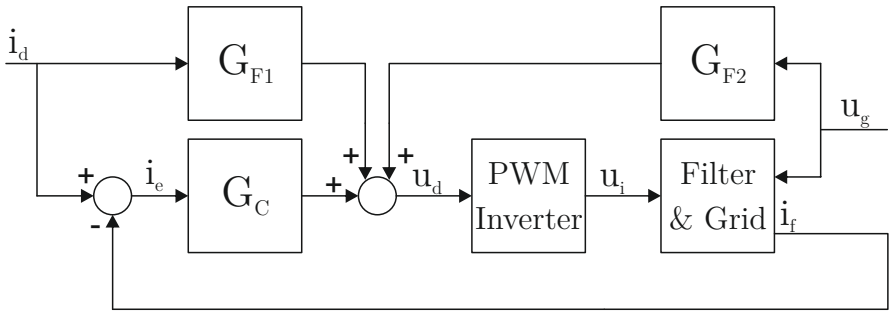


FIGURE 5.1: Architecture of PWM controller with feedback and feed-forward control blocks

i_e, which is the difference between the desired current i_d and the measured filter current i_f, to determine its contribution to the desired grid voltage u_d.

The two feed-forward controllers G_{F1} and G_{F2} can be designed if the properties of the LCL filter are known. G_{F1} estimates the required inverter voltage u_i needed to feed in the desired current i_d into the grid. G_{F2} estimates the inverter voltage needed to compensate for the effect of the grid voltage. The advantage of using feed-forwards controllers is that they can compensate for the error current in advance, before it appears, whereas the feedback controller only reacts to an error which is already present [48]. If the feed-forward controllers are effective, the error current i_e can be reduced, improving the quality of the currents fed into the grid.

5.2 Controller Development

To design a controller based on the architecture presented in Figure 5.1, we start by creating a state-space representation of the LCL filter. The schematic diagram of the inverter was presented in Figure 4.1 on page 32. The nodal equations describing the system, ignoring the ESR of the capacitor, are:

$$i_f = i_g + i_c \tag{5.1}$$

$$i_c = C_f \frac{du_c}{dt} \tag{5.2}$$

$$u_i - u_c = R_{fi}\, i_f + L_{fi}\, \frac{di_f}{dt} \tag{5.3}$$

$$u_c - u_g = R_{fg}\, i_g + L_{fg}\, \frac{di_g}{dt} \tag{5.4}$$

The equations can be transformed to create a state space representation of the system:

$$\frac{d}{dt} i_f = -\frac{R_{fi}}{L_{fi}} i_f - \frac{1}{L_{fi}} u_c + \frac{1}{L_{fi}} u_i \tag{5.5}$$

$$\frac{d}{dt} i_g = -\frac{R_{fg}}{L_{fg}} i_g + \frac{1}{L_{fg}} u_c - \frac{1}{L_{fg}} u_g \tag{5.6}$$

$$\frac{d}{dt} u_c = \frac{1}{C_f} i_f - \frac{1}{C_f} i_g \tag{5.7}$$

In matrix form, using the standard state space representation $\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u}$, the equations take the following form:

$$\begin{bmatrix} \dot{i}_f \\ \dot{i}_g \\ \dot{u}_c \end{bmatrix} = \begin{bmatrix} -\frac{R_{fi}}{L_{fi}} & 0 & -\frac{1}{L_{fi}} \\ 0 & -\frac{R_{fg}}{L_{fg}} & \frac{1}{L_{fg}} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} i_f \\ i_g \\ u_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{fi}} & 0 \\ 0 & -\frac{1}{L_{fg}} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} u_i \\ u_g \end{bmatrix} \tag{5.8}$$

The output of the system takes the general form $\dot{\mathbf{y}} = \mathbf{C}\mathbf{x} + \mathbf{D}\mathbf{u}$. The state variables are also the output variables, $\mathbf{y} = \mathbf{x}$. With the sensors installed in the Mobile VISMA hardware, it is possible to measure all states of the system.

There are two inputs to the system, the inverter voltage u_i and the grid voltage u_g. The system is a Multiple-Input and Multiple-Output (MIMO) system, but the only input value that can be controlled is u_i.

5.2.1 Feedback system design

Based on the state space model of the system, we can obtain transfer functions which relate the output of the system to the system inputs. For the design of the feedback controller G_C, the following transfer functions are of interest:

$$G_{1f}(s) = \frac{I_f(s)}{U_i(s)} \tag{5.9}$$

$$G_{1g}(s) = \frac{I_g(s)}{U_i(s)} \tag{5.10}$$

The transfer function $G_{1f}(s)$ relates the filter current i_f to the inverter voltage u_i, whereas $G_{1g}(s)$ relates the grid current i_g to the inverter voltage u_i. The transfer functions have the form:

$$G_1(s) = \frac{I_g(s)}{U_i(s)} = \frac{a_2\, s^2 + a_1\, s + a_0}{s^3 + b_2\, s^2 + b_1\, s + b_0} \tag{5.11}$$

Substituting numeric values for the filter component parameters, the transfer functions become:

$$G_{1f}(s) = \frac{333.3\, s^2 + 33.3 \cdot 10^3\, s + 2.2 \cdot 10^{10}}{s^3 + 166.7\, s^2 + 8.9 \cdot 10^7\, s + 6.7 \cdot 10^9} \tag{5.12}$$

$$G_{1g}(s) = \frac{2.2 \cdot 10^{-12}\, s^2 + 2.2 \cdot 10^{10}}{s^3 + 166.7\, s^2 + 8.9 \cdot 10^7\, s + 6.7 \cdot 10^9} \tag{5.13}$$

Figures 5.2 and 5.3 show the root locus diagrams of the transfer function G_{1f} and G_{1g}, respectively. The closed-loop poles of the transfer function G_{1f} are all negative, indicating that the system is stable, whereas the transfer function G_{1g} has positive closed-loop poles, which make the system unstable already for small values of the proportional gain K_p. Because of this, i_g cannot be used for feedback. Instead, i_f can be used as the feedback variable in the control system, and i_g can be expected to track i_f closely under normal operating conditions.

The control problem of feeding a current into the grid through an LCL filter is analogous to the velocity control problem of a motor driving a load, where the load is connected to the motor through an elastic coupling, as shown in Figure 5.4. This problem was described in [49], where it was shown that velocity control of the load is not possible using the measured velocity of the load as feedback, but can be done using the motor velocity as feedback. The transfer functions of the

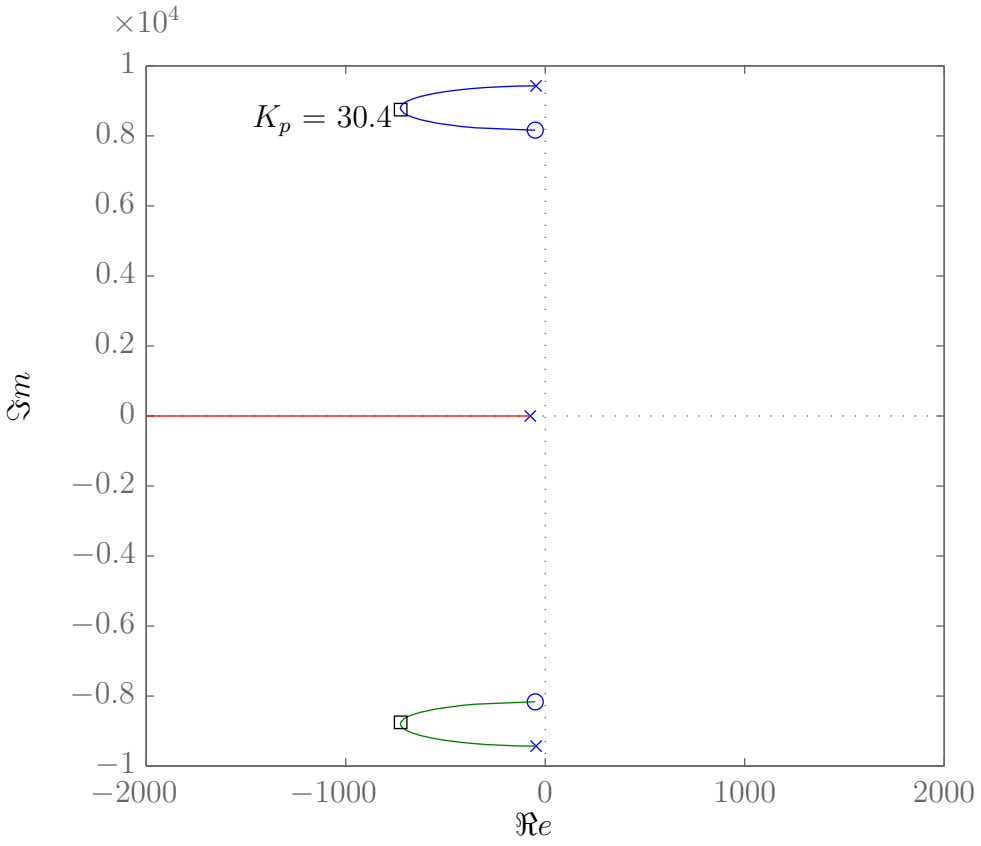


FIGURE 5.2: Root locus of closed-loop system with the open-loop transfer function G_{1f}.

mechanical system have the same form as the transfer functions of the LCL filter. For the mechanical system, [49] provides an analytical solution to the problem of finding the optimal proportional gain $\mathrm{K_{p\,opt}}$ and integrator time constant T_n of a PI feedback controller for a system with an open-loop transfer function analogous to G_{1f}. This solution can be applied to the electrical system as well. For the transfer function of the mechanical system with no damping:

$$G_m(s) = \frac{1}{\theta\lambda} \cdot \frac{s^2 + \lambda {\omega_0}^2}{s^2 + {\omega_0}^2} \tag{5.14}$$

where ω_0 is the resonance frequency of the system, θ is the total inertia of the system, and λ is the ratio of the motor inertia to the total system inertia, the value of the proportional gain, for which the damping is optimal [50, 51], is:

$$\mathrm{K_{p\,opt}} = \lambda^{0.75}\omega_0\theta \tag{5.15}$$

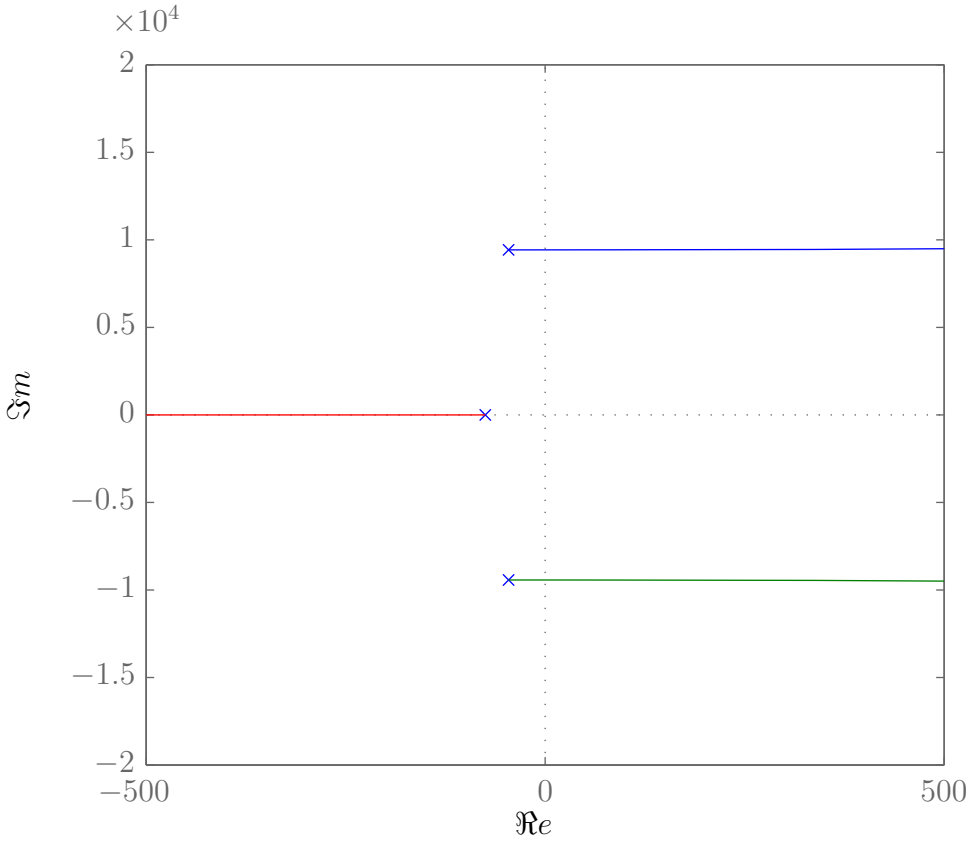


FIGURE 5.3: Root locus of closed-loop system with the open-loop transfer function G_{1g}

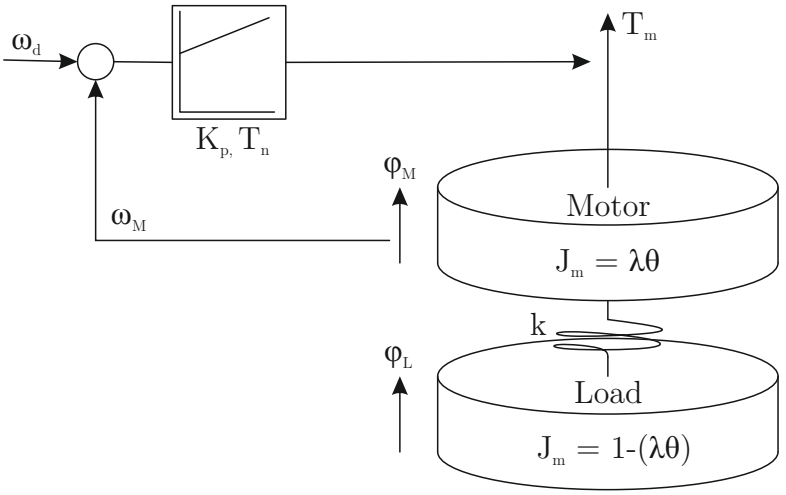


FIGURE 5.4: Mechanical system analogous to the electrical inverter system [49]. Velocity control of the motor is performed using a PI feedback controller.

and the integrator time constant T_n is [49]:

$$T_n = \frac{4}{\omega_0 \lambda^{0.75}} \tag{5.16}$$

Knowing T_n, for a PI controller with the transfer function $G_C = K_p + K_i/s$, the value of the integral component K_i can be calculated as:

$$\mathrm{K_i} = \frac{1}{4}\,\lambda^{1.5}\omega_0^2\theta \tag{5.17}$$

To apply these results to the LCL filter, let us start with the transfer function G_{1f}. Ignoring the internal resistance of the components, G_{1f} can be written in a form equivalent to that of the mechanical transfer function (5.14)

$$\begin{aligned} G_{1f}(s) \overset{R_f,R_g\to 0}{=} \frac{U_g(s)}{I_f(s)} &= \frac{1}{\theta\lambda}\cdot\frac{s^2+\lambda{\omega_0}^2}{s^2+{\omega_0}^2} \\ &= \frac{1}{sL_{fi}}\cdot\frac{s^2+\frac{1}{L_{fg}C}}{s^2+\frac{L_{fi}+L_{fg}}{L_{fi}L_{fg}C_f}} \end{aligned} \tag{5.18}$$

For the LCL filter, ω_0 is the resonance frequency, θ is the total inductance of the system, and λ is the ratio of the inverter site filter inductance L_{fi} to the total system inductance θ.

$$\theta = L_{fi} + L_{fg} \tag{5.19}$$

$$\lambda = \frac{L_{fi}}{\theta} \tag{5.20}$$

$$\omega_0 = \sqrt{\frac{\theta}{L_{fi}L_{fg}C_f}} \tag{5.21}$$

The optimal proportional gain for the feedback controller can be calculated using (5.15):

$$\mathrm{K_{p\,opt}} = \lambda^{0.75}\omega_0\theta = 30.4\,\mathrm{V/A} \tag{5.22}$$

and the integral gain can be calculated using (5.17):

$$\mathrm{K_i} = \frac{1}{4}\,\lambda^{1.5}\omega_0^2\theta = 57,775\,\mathrm{V/As} \tag{5.23}$$

In Figure 5.2, the imaginary poles for the optimal gain are marked on the plot as black squares. The application of (5.22) to various servoaxes has shown that the controller commissioning is quite robust [51]. The system parameters ω_0, λ, and θ may vary around 40% without destabilizing the control performance.

One problem with using i_f for feedback is the large amount of current ripple present on i_f due to the switching nature of the inverter. It is of advantage to keep the proportional gain of the feedback controller low, so as not to amplify the noise in the system.

Figure 5.5 shows the desired voltages u_d, the PWM carrier signal u_c, and the PWM output signal for an inverter using a proportional controller with gain $K_p = 30\,\mathrm{V/A}$ (TOP) and $K_p = 120\,\mathrm{V/A}$ (BOTTOM) feeding a current into a short-circuit. The gain should be set so that the rate of change of the desired voltage is smaller than the rate of change of the carrier signal, in which case the carrier signal and the desired voltage will intersect twice per switching period, creating an output PWM signal with a fixed frequency (see TOP graph). If the proportional gain is too high (see BOTTOM graph), the desired voltage u_d calculated by the controller and the carrier signal u_c overlap in several places during one period of the carrier signal, creating a faulty, high-frequency PWM output signal. The calculated optimal system gain $\mathrm{K_{p\,opt}} = 30.4\,\mathrm{V/A}$ is sufficiently small, and does not cause problems.

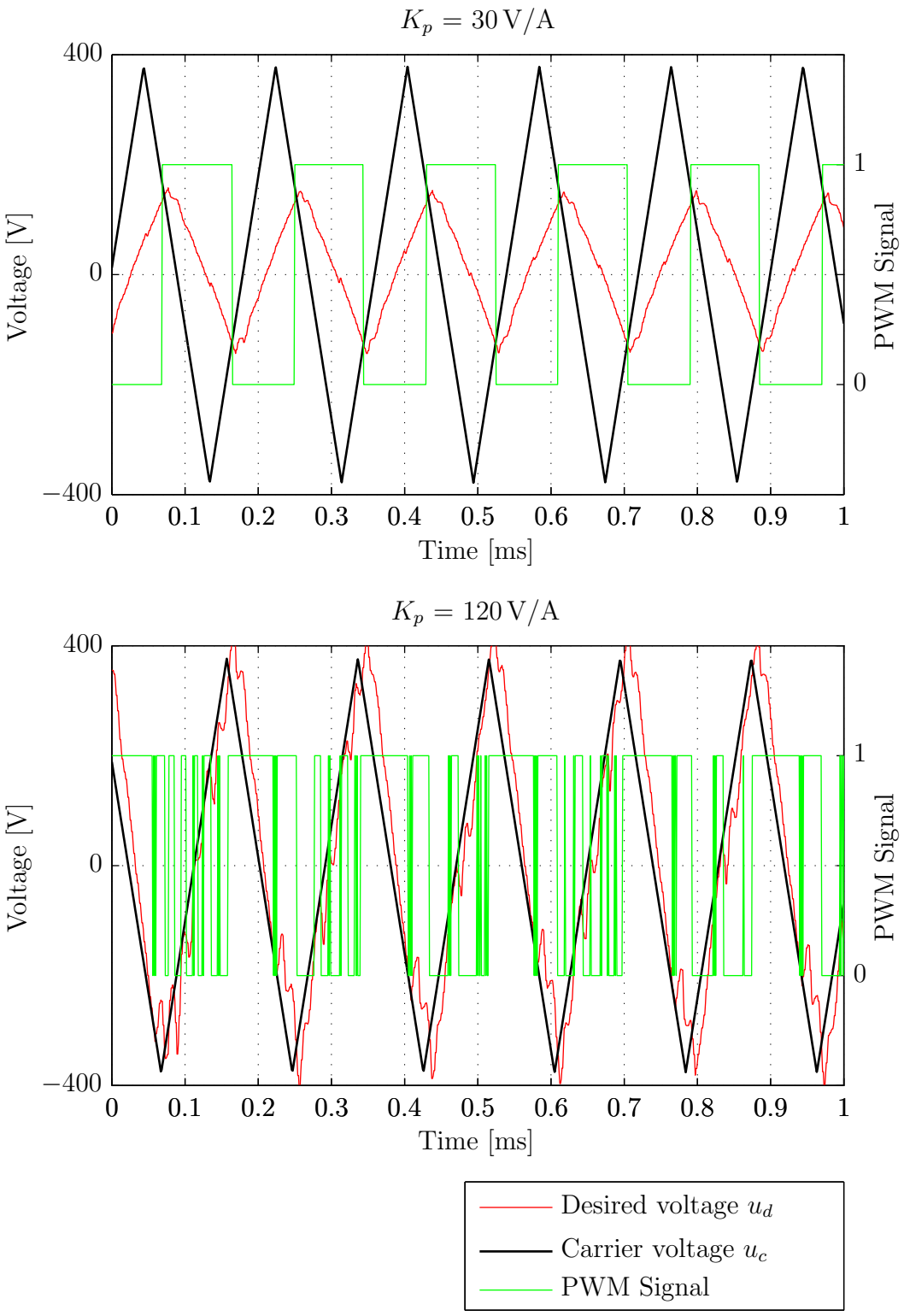


FIGURE 5.5: PWM carrier signal u_c and desired voltage u_d for inverter feeding a current into the grid using a proportional controller with $K_p = 30\,\mathrm{V/A}$ (TOP) and $K_p = 120\,\mathrm{V/A}$ (BOTTOM). An excessively high proportional gain (BOTTOM) causes the carrier and desired voltages to overlap and results in a high-frequency output PWM signal.

5.2.2 Controller design using a simplified simulation model

For designing the feed-forward controllers, a simplified PLECS model of the inverter system was created, where the inverter was replaced by a controllable voltage source with linear output, as shown in Figure 5.6.

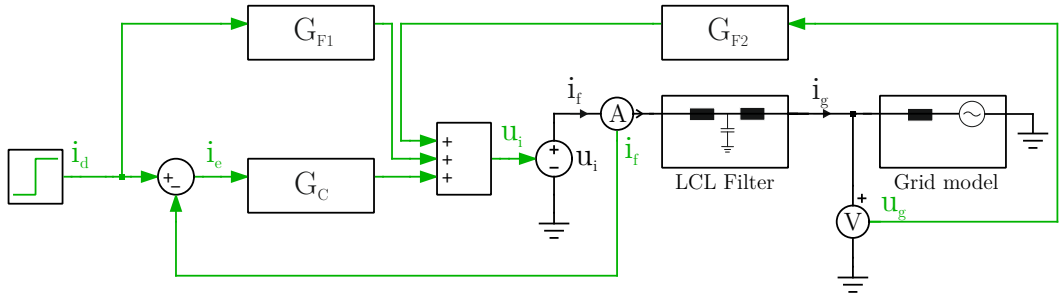


FIGURE 5.6: PLECS model of the PWM current controller with the inverter replaced by a controllable voltage source

Let us consider the case where the grid voltage $u_g = 0$ and design the feed-forward controller G_{F1}. For this, the transfer function $G_{1g}(s)$ should be considered. The gain of G_{F1}, K_{F1}, is the inverse of the gain of the transfer function $G_{1g}(s)$.

$$K_{F1} = \frac{1}{\lim_{s\to 0} G_{1g}} \tag{5.24}$$

While $G_{1g}(s)$ behaves like a first-order lag element and is stable, the open-loop step response of the transfer function is slow. The settling time of $G_{1g}(s)$ is 52 ms, so a proportional feed-forward controller alone is too slow for feeding a sine current with a period of 20 ms into the grid.

To increase the speed of response of the feed-forward controller, a phase-lead compensator can be used. The lead compensator has the transfer function [52]:

$$G_L = \frac{1 + a\tau s}{1 + \tau s} \tag{5.25}$$

where $a > 1$. The compensator adds positive phase to the system between corner angular frequencies at $\omega_{c1} = 1/\tau$ and $\omega_{c2} = 1/(a\tau)$ and increases the gain at high frequencies.

In Figure 5.7, the bode plots of two controllers are compared, a proportional feed-forward controller (BLUE) with the transfer function $G_{F1}(s) = K_{F1}$ and a

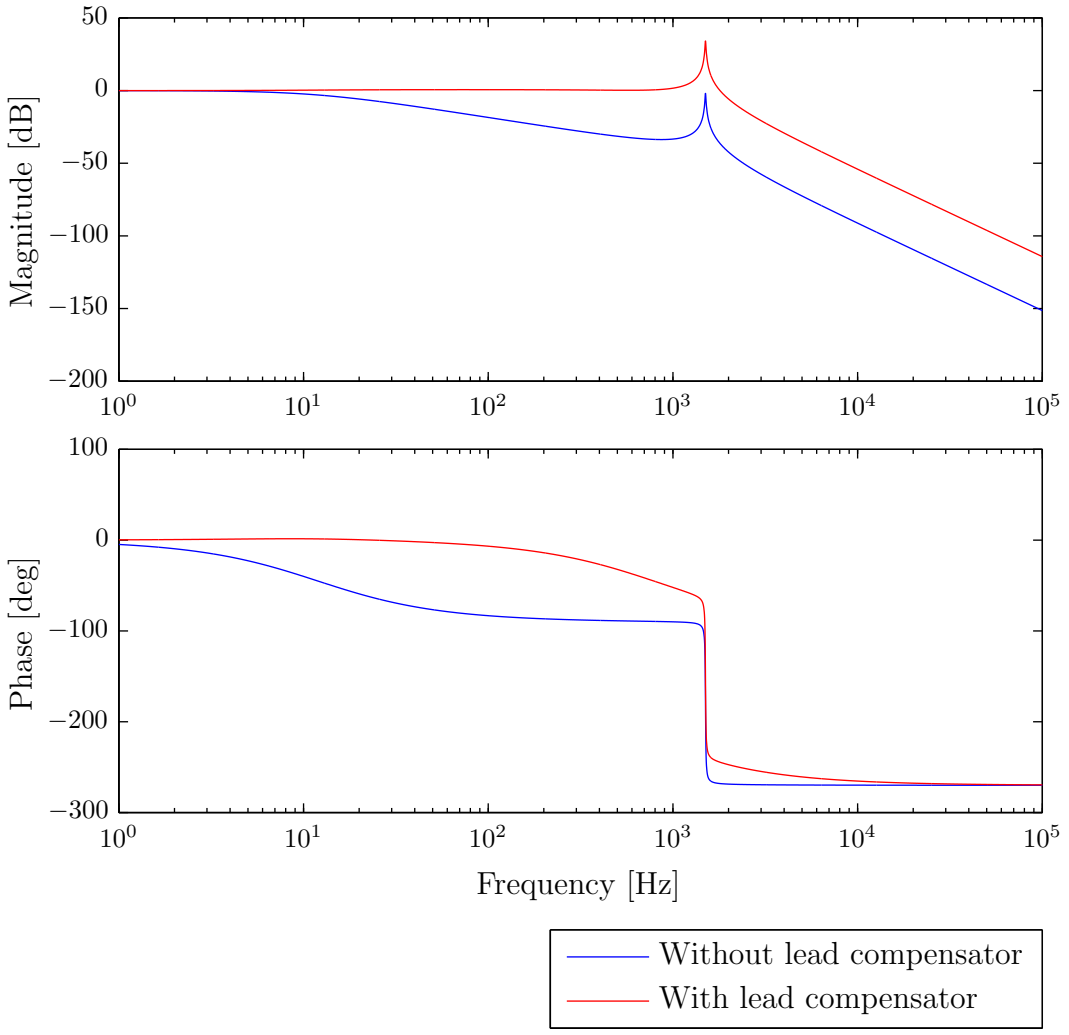


FIGURE 5.7: Bode plot of system controlled by feed-forward controller G_{F1} with and without a phase-lead compensator.

feed-forward controller with a phase-lead compensator (RED) with the transfer function:

$$G_{F1}(s) = K_{F1}\frac{1+a\tau s}{1+\tau s} \tag{5.26}$$

The parameters chosen for the controllers were:
$K_{F1} = 0.3$, $a = 72$, and $\tau = 2.5 \cdot 10^{-3}$.

The system controlled by a proportional controller without the phase-lead compensator has a $-3\,\text{dB}$ bandwidth of around 12 Hz and a large phase shift. The high-frequency gain introduced by the phase-lead compensator stabilizes the gain of the controlled system, bringing it near unity for frequencies up to around 0.5 kHz. The phase-lead compensator also has the positive effect of significantly reducing the

phase shift for low frequencies in the controlled system. The increased response speed and reduced phase shift created by the phase-lead compensator makes it suitable for the feed-forward controller G_{F1}, allowing the controller to feed a 50 Hz current into the grid.

The robustness of the feed-forward controller G_{F1} can be examined by observing the bode plot of the controlled system when the parameters of the system are varied but the parameters of the feed-forward controller are kept constant. In the design of the feed-forward controller G_{F1}, we only considered the transfer function of the LCL filter, so the performance will be investigated for variations in parameters of the passive components used in the LCL filter (see Section 4.2.2).

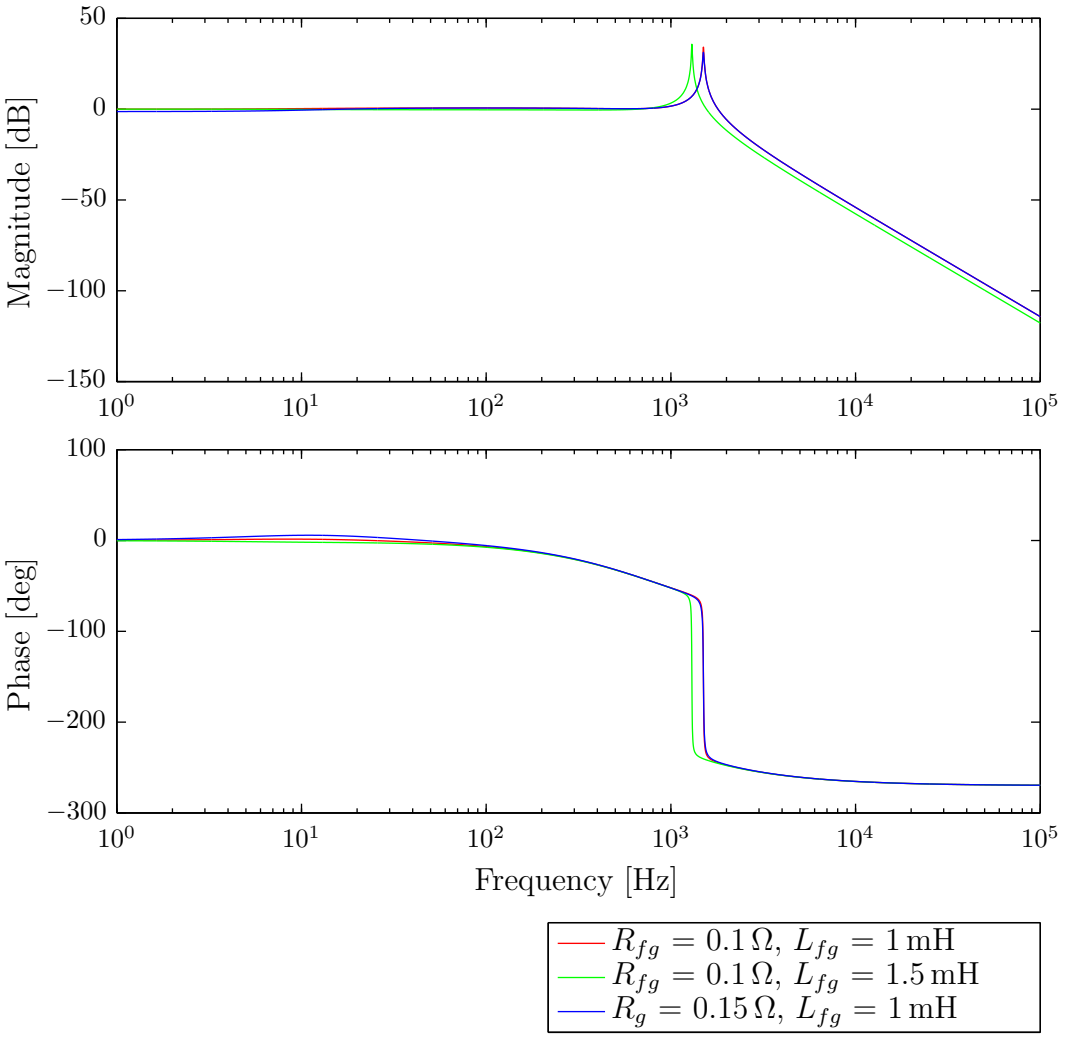


FIGURE 5.8: Bode plot of system controlled by feed-forward controller G_{F1} with phase-lead compensator for different values of inducance and internal resistance of the grid-side filter inductor

Figure 5.8 shows the bode plots of a system controlled by G_{F1} for different parameters of the grid-side inductor. Changes in the internal resistance of the inductor cause a change in the open-loop gain of the controlled system, which makes the feed-forward controller less effective. A higher inductance in the current path reduces the open-loop gain for higher frequencies and reduces the resonance frequency of the system. The same effect is observed if the inverter-side inductor impedance is changed. Although variations in the system parameters reduce the effectiveness of the feed-forward controller, such a controller may still be beneficial if used in combination with a feedback controller.

The next step is to consider the effect of the grid voltage on the system and design the feed-forward controller G_{F2} to compensate for it. Under DC conditions, if $u_i = u_g$, there would be no current flowing between the filter and the grid, i.e. $i_g = 0$. Assuming the DC conditions were true, a proportional controller $G_{F2}(s) = 1$ would completely compensate the effect of the grid voltage. Since u_i

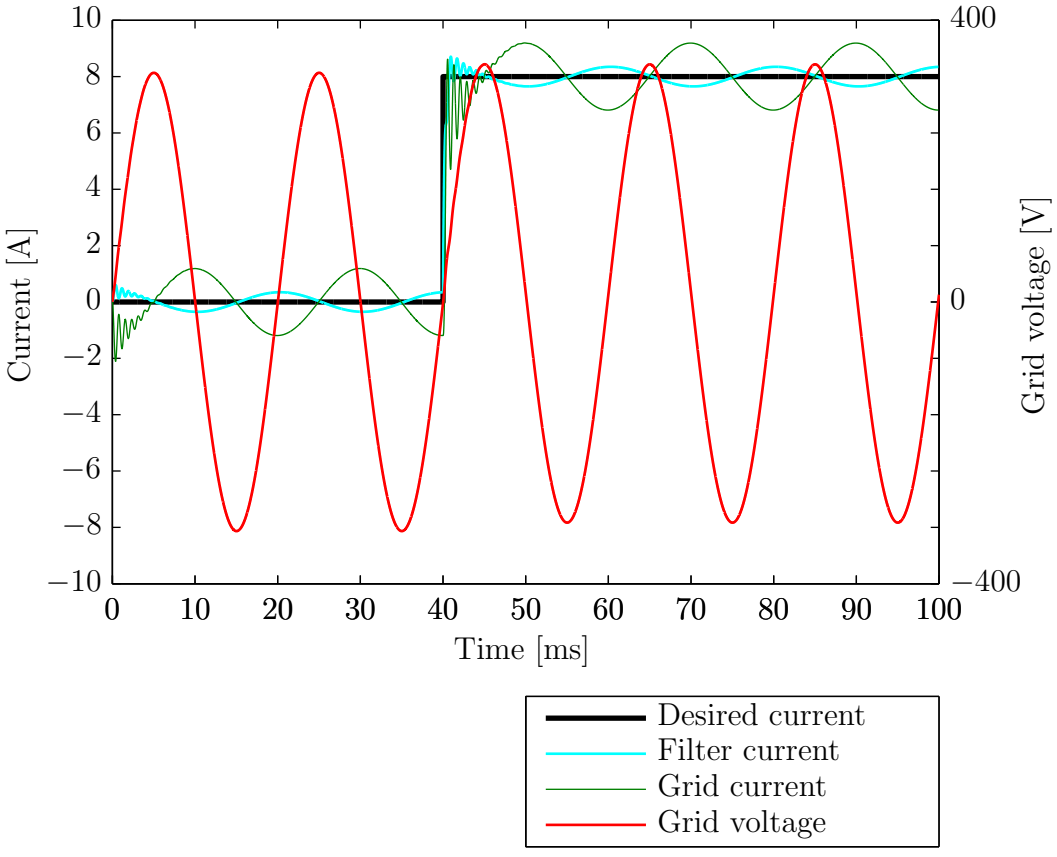


FIGURE 5.9: Step response of system controlled by feed-forward controllers G_{F1} and G_{F2}

is an AC voltage, using this feed-forward controller, some current will flow into the capacitor of the LCL filter.

Figure 5.9 shows the step response of the system connected to the grid with both feed-forward controllers G_{F1} and G_{F2} implemented, but the feedback controller G_C disabled. The proportional feed-forward controller G_{F2} is not able to completely compensate for the effect of the grid voltage, and a residual grid current with an amplitude of 1.2 A remains, which lags the grid voltage by 90 degrees. Knowing the amplitude of this residual grid current, which can be measured while the inverter is switched off, and the angle by which it lags the grid voltage, an additional compensator G_{F3} can be implemented which adds the inverse of the expected residual current to the desired current.

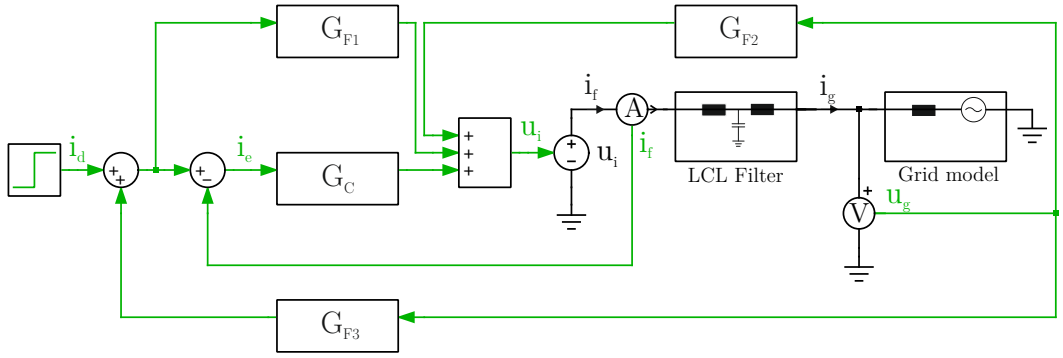


FIGURE 5.10: PLECS model of a PWM current controller with the inverter replaced by a controllable voltage source with an additional grid voltage compensation controller G_{F3}

Figure 5.10 shows a simulation model of the system with the additional compensator G_{F3}. G_{F3} calculates the expected residual current based on the measured grid voltage. G_{F3} can be either implemented as a PLL which synchronizes with the grid voltage and outputs a sine wave lagging the voltage 90 degrees in phase, or as an all-pass filter that introduces a 90-degree phase shift. The transfer function of G_{F3} implemented as an all-pass filter is:

$$G_{F3}(s) = \frac{1}{K_{F3}} \frac{\tau s - 1}{\tau s + 1} \tag{5.27}$$

where K_{F3} is the gain and τ is the inverse of the angular frequency for which the phase shift is 90 degrees. The gain K_{F3} is set so that the amplitude of the output signal is equal to the amplitude of the expected residual current.

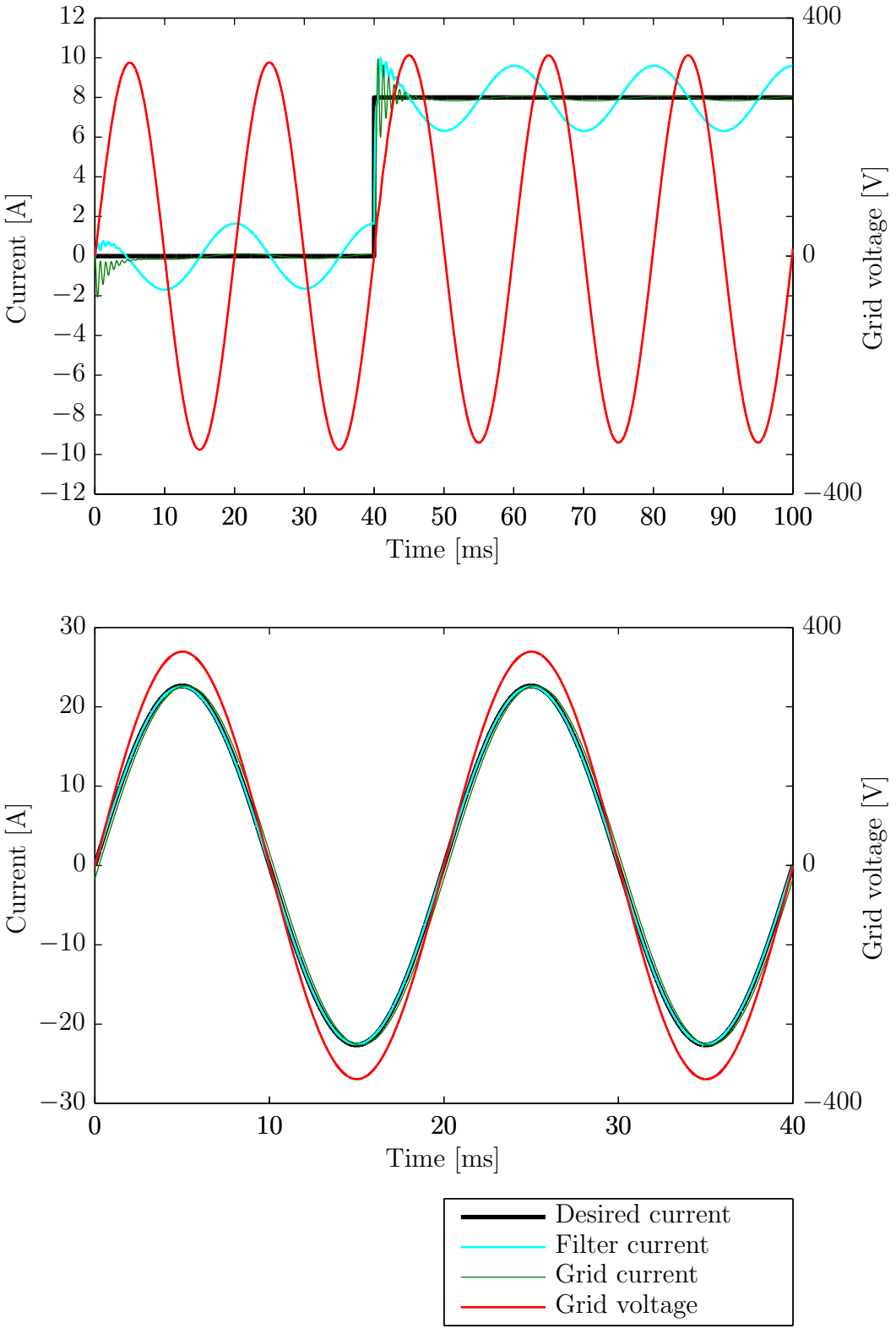


FIGURE 5.11: Simulation of step current(TOP) and sinusoidal current (BOTTOM) fed into the grid using an inverter controlled by feed-forward controllers G_{F1}, G_{F2} and an additional grid voltage compensator G_{F3}

Figure 5.11 shows the response of the system without a feedback controller using the feed-forward controllers G_{F1}, G_{F2}, and G_{F3} to feed in a current with the form of a step function (TOP) and 16 A sinusoidal current (BOTTOM) into the grid. In the step response it can be seen that, with the additional controller G_{F3}, the effect of the grid voltage is totally compensated. The results of both simulations show that if the system parameters are known precisely, feed-forward controllers alone are successful at feeding a current into the grid.

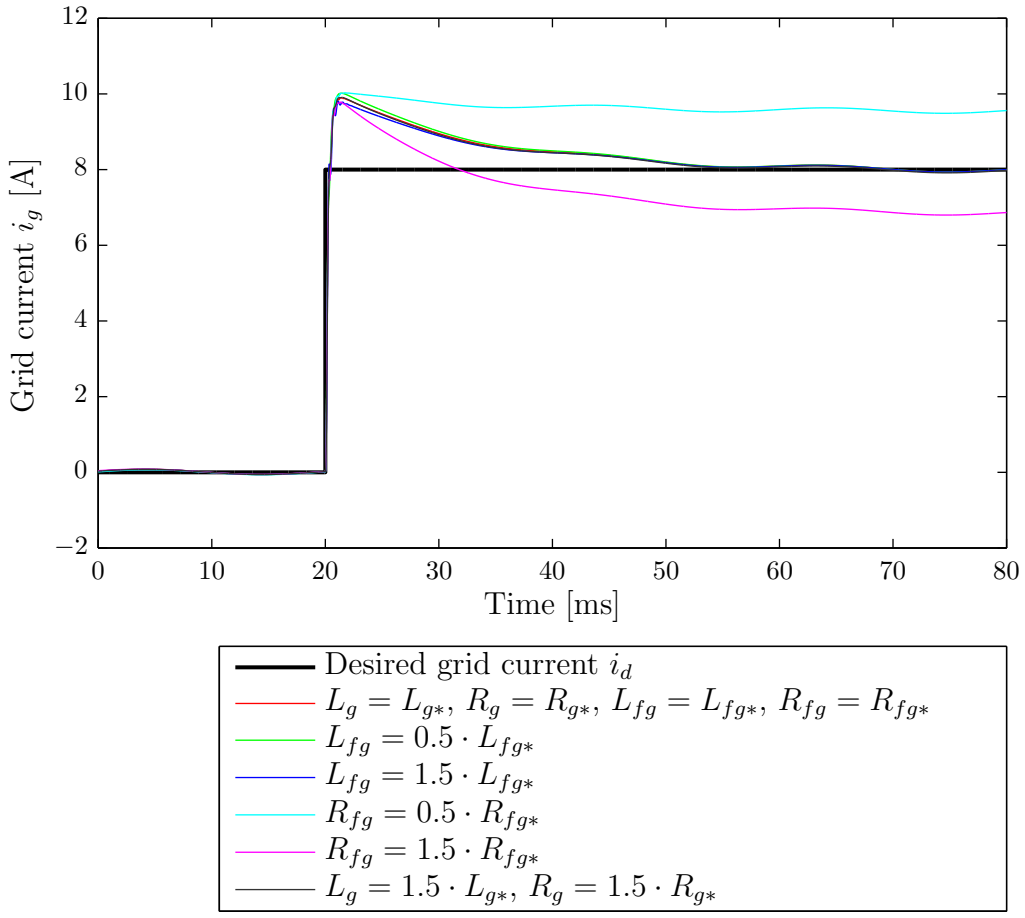


FIGURE 5.12: Simulated step response of system controlled only by feed-forward controllers G_{F1},G_{F2}, and G_{F3}, when the grid and filter parameters vary from the grid and filter parameters (denoted with $*$ subscript) used to find the feed-forward controller parameters.

To examine the robustness of the feed-forward controllers, let us consider Figure 5.12, which shows the simulated step response of the system without a feedback controller that uses only the feed-forward controllers G_{F1}, G_{F2}, and G_{F3} to feed a current into the grid for different values of the filter and grid parameters. The

feed-forward controller parameters were calculated for the filter and grid parameters denoted with the $*$ subscript. The results of the simulation show that the performance of the feed-forward controlled system is not degraded by variations of grid parameters, i.e. the resistance and inductance of the power lines, nor by variations of the LCL filter inductances. The feed-forward controller is however sensitive to variations in the internal resistances of the inductive components of the LCL filter, since the feed-forward controller gain is based on the components' resistance values. Although on their own, the feed-forward controllers cannot be relied upon to feed the desired currents into the grid because of variations in system parameters, when operating in parallel with a feedback controller, they should be able to improve control performance.

5.2.3 Simulation model of the PWM-controlled system

Until now, the control system designed in this chapter has been tested in simulations which assumed that linear control of the inverter voltage is possible. Now the controllable voltage source can be replaced by a PWM-controlled IGBT inverter.

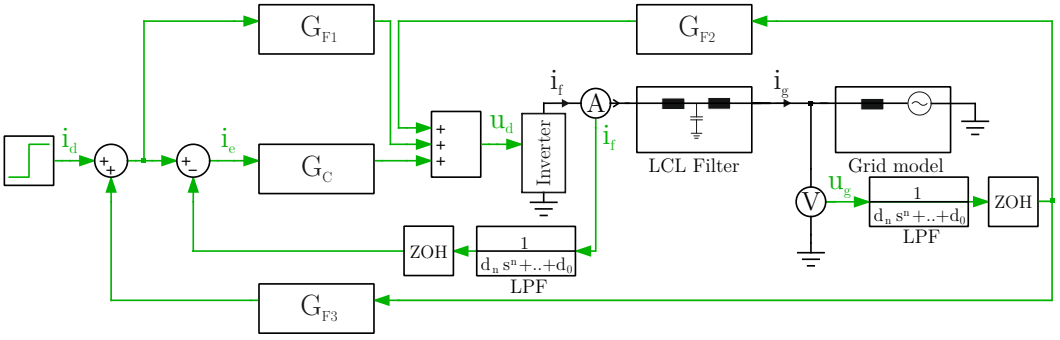


FIGURE 5.13: PLECS model of the inverter system with a PWM-based current controller

In Chapter 4 a simulation model of the inverter was created in PLECS and verified with experiments using the hysteresis current controller. For the hysteresis current controller, results obtained from simulation were consistent with reality, so the simulation model can be used for testing the PWM controller prior to implementation in hardware.

Figure 5.13 shows a model of the system with the PWM-controlled inverter. The inverter block contains a model of the IGBT inverter and PWM modulator. The

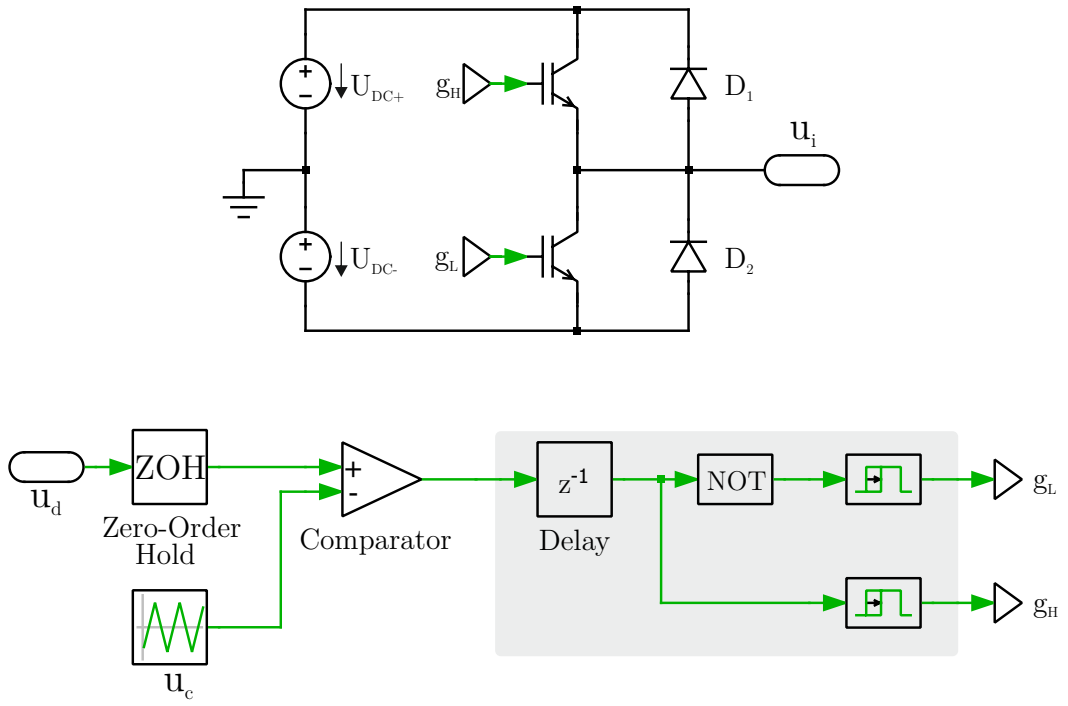


FIGURE 5.14: PLECS model of a PWM-controlled inverter leg comprising a PWM modulator, gate drivers with dead-time generation, and an IGBT inverter leg

internal design of the block is shown in Figure 5.14. The input to the block is the desired inverter output voltage, and the output is the electrical connection to the inverter leg output. The PWM modulator in the inverter block takes as input the desired inverter output voltage and outputs the PWM switching signal, which serves as an input to the IGBT driver. In the system model, the LPF and ZOH blocks are used to model the anti-aliasing filters and ADC sampling, respectively.

With the simulation model in place, the PWM controller could be tested. First, the PWM controller was tested with the feedback controller disabled to verify whether the designed feed-forward controllers would have the same regulating effect on the system with the PWM-controlled inverter as they did on the system with the controlled voltage source. In the simulation, a symmetrical triangular carrier wave with a frequency of $f_c = 11\,\text{kHz}$ was used for the PWM modulator. The IGBT deadtime was set to $T_d = 4\,\text{us}$, the minimum for the IGBTs used in the Mobile VISMA. Figure 5.15 shows the step response of the system when feeding a current with the form of a step function into a short circuit. Clearly, the system fails to feed in the desired current.

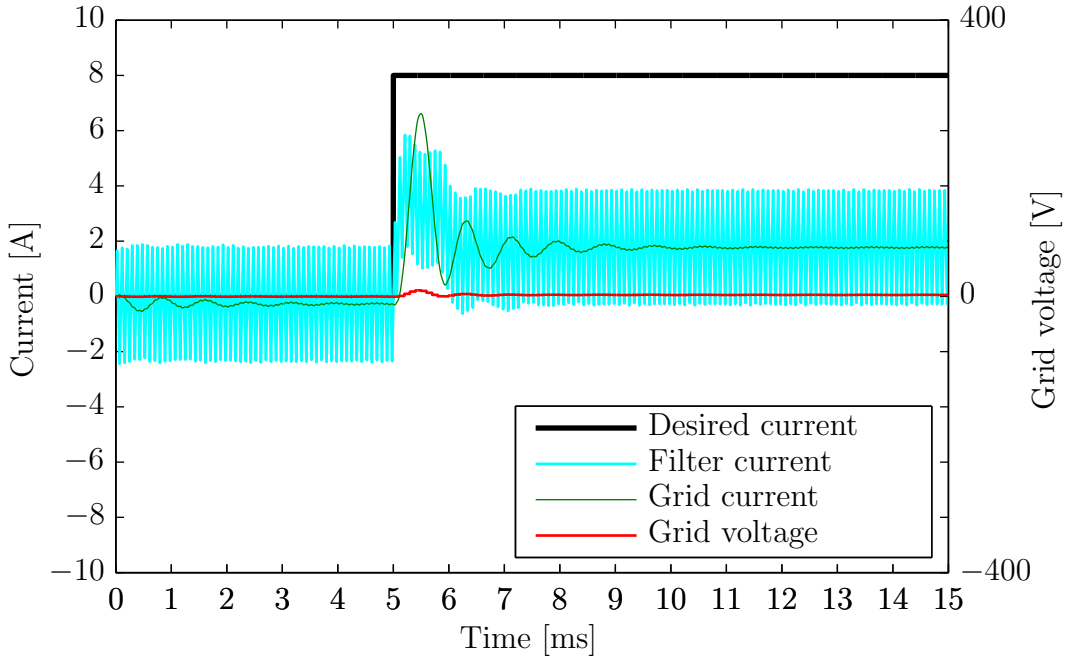


FIGURE 5.15: Step response of PWM inverter without dead-time compensator controlled by feed-forward controllers G_{F1}, G_{F2} and additional grid voltage compensator G_{F3} when feeding current into a short circuit. The dead-time creates an error in the inverter output voltage; the result is that the inverter fails to feed in the desired current.

5.2.4 Deadtime compensation in the PWM Inverter

Simulations were performed to find the reason why the PWM inverter with feed-forward controllers failed to feed in the desired current. The problem was traced to the deadtime. If the deadtime in the simulation model is removed, the feed-forward current control performance improves significantly. Using faster IGBTs alone would not solve the problem, as the deadtime would have to be reduced by two orders of magnitude to approx. 50 ns to get acceptable results. Even with the fastest IGBTs, this is not possible.

In [53] the effect and modeling of deadtime in PWM voltage inverters was thoroughly discussed, and a deadtime compensation method was developed. During the deadtime, the output voltage of the inverter, u_i, depends on the inductive current i_f. If i_f is positive, the freewheeling diode of the bottom IGBT switches on, and the inverter output voltage becomes equal to the negative DC-link voltage, $u_i = -U_{DC}$. If i_f is negative, during deadtime the free-wheeling diode of the top IGBT switches on, and the inverter output voltage becomes equal to the positive

DC-link voltage, $u_i = U_{DC}$. Based on this behavior of an inverter during the deadtime, in [53] a model of an inverter was created which takes into account the deadtime, and an effective deadtime compensation method was designed. This compensation method requires the knowledge of the switching element (IGBT) parameters, but is not affected by changes in parameters of the load. The inverter model and deadtime compensator developed in [53] are reproduced in Figure 5.16. The deadtime compensator consists of two blocks, $g(i_f)$, which evaluates the direction of current flow, and $f(\hat{e})$, which is a hysteresis function that takes as input $\hat{e}$, which is the difference between the desired voltage u_d and the PWM carrier signal u_c, and outputs the compensation signal $f(\hat{e})$. The output of the compensator $f(\hat{e})$ can take two different values, $\epsilon/2$ or $-\epsilon/2$, where

$$\epsilon = 4 f_c T_d U_c \tag{5.28}$$

and f_c, T_d, and U_c are the PWM carrier frequency, deadtime, and carrier signal amplitude (1/2 of the carrier peak-to-peak voltage), respectively. A PLECS simulation model of the inverter with the deadtime compensator is shown in Figure 5.17.

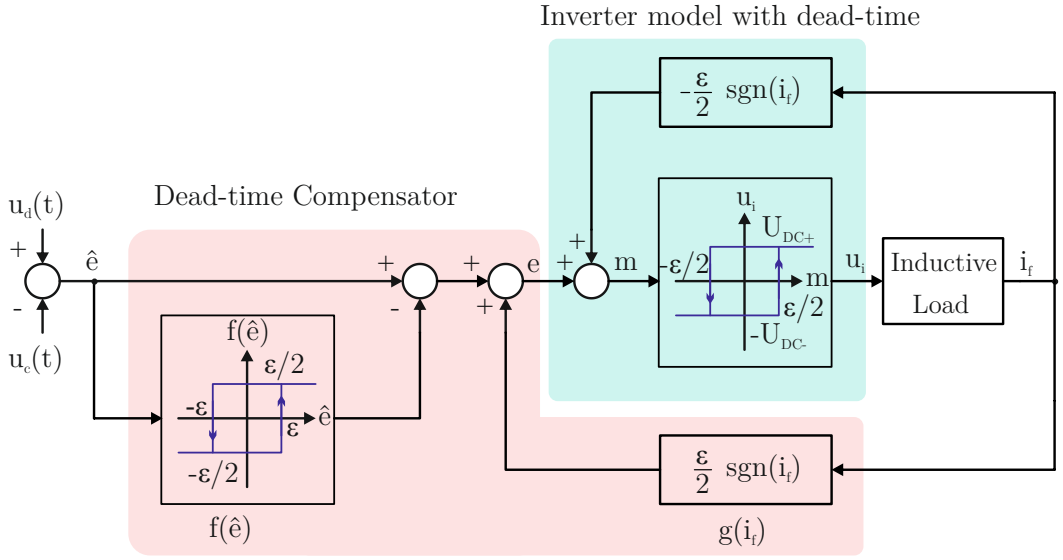


FIGURE 5.16: Model of inverter with dead-time and dead-time compensator as proposed in [53]

Figure 5.18 shows the response of the system with the deadtime compensator when feeding a current with the form of a step function into a short circuit. The results show an improvement over the system without a compensator (compare to Figure 5.15).

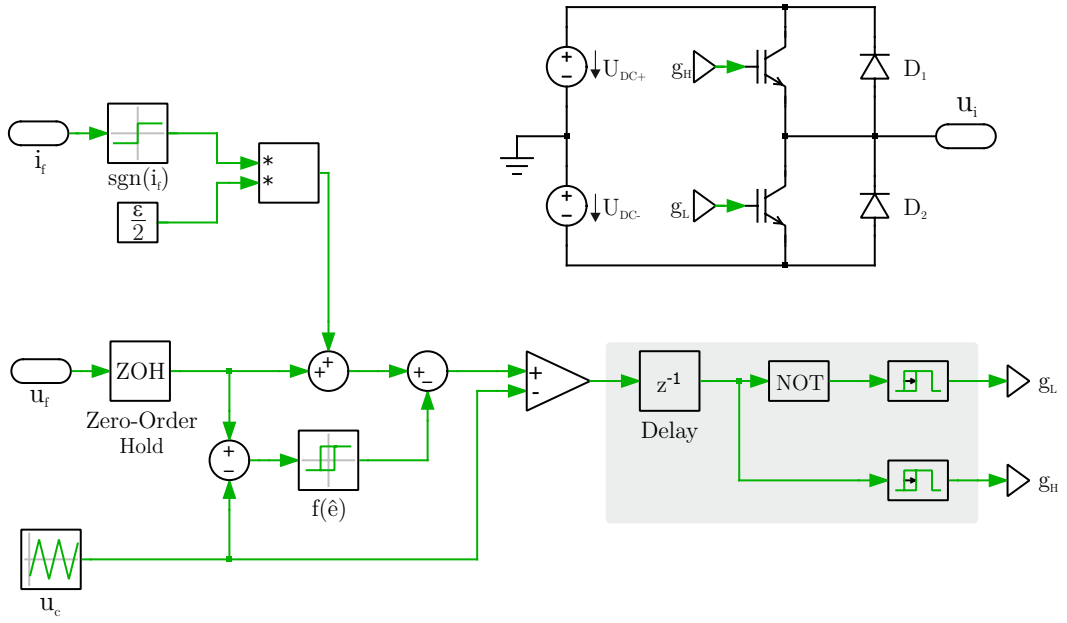


FIGURE 5.17: PLECS model of PWM inverter with dead-time compensator

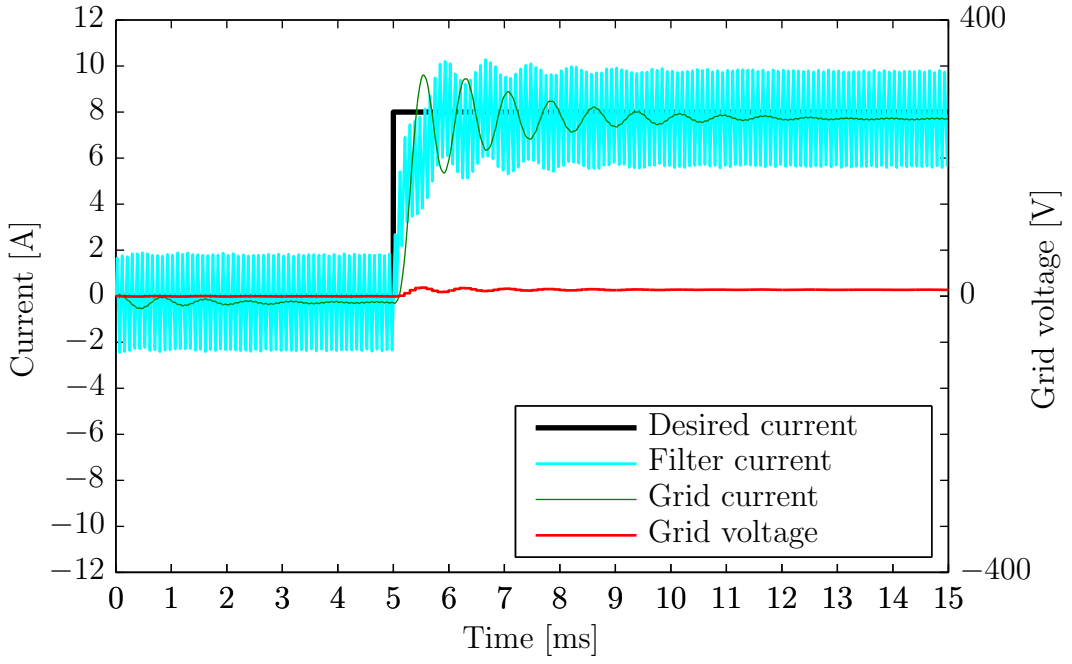


FIGURE 5.18: Response of PWM inverter with dead-time compensator controlled by feed-forward controllers G_{F1}, G_{F2} and additional grid voltage compensator G_{F3} feeding a current with the form of a step function into a short circuit.

Further simulations have shown, when feeding a current into the grid, even with the deadtime compensator, the PWM inverter fails to feed in the desired currents when using feed-forward controllers alone if the deadtime T_d is too long. During one period of the PWM carrier signal, $T_c = 1/f_c$, the deadtime occurs twice. The deadtime ratio

$$DT_{\%} = \frac{2T_d}{T_c} \cdot 100\% \tag{5.29}$$

is the percent of time spent by the inverter in the state where both IGBTs are off per period of the PWM carrier signal. For $T_d = 4\,\mu$s and $f_c = 11\,$kHz, $DT_{\%} = 8.8\%$.

Figure 5.19 shows the results of simulations, where a sinusoidal current with an RMS value of 16 A is fed into the grid. In the top figure, the simulation results are shown for a fixed PWM carrier frequency of $f_c = 11\,$kHz and different deadtimes. In the bottom figure, simulation results are shown for a fixed deadtime of $4\,\mu$s and different carrier frequencies. For current traces in the top and bottom plots having the same color, the deadtime ratios $DT_{\%}$ are equal. By comparing the top and bottom plots, it can be seen that a low deadtime ratio is important for good feed-forward controller performance, which can be achieved by lowering the PWM carrier frequency or decreasing the deadtime.

The inverter used in the Mobile VISMA allows a minimum dead time of $4\,\mu$s. The simulations show good feed-forward controller performance for a deadtime of $T_d = 2\,\mu$s at $f_c = 11\,$kHz ($DT_{\%} = 4.4\%$). Reducing the carrier frequency to $f_c = 5.5\,$kHz improves the feed-forward performance, but also increases the ripple in the filter current i_f.

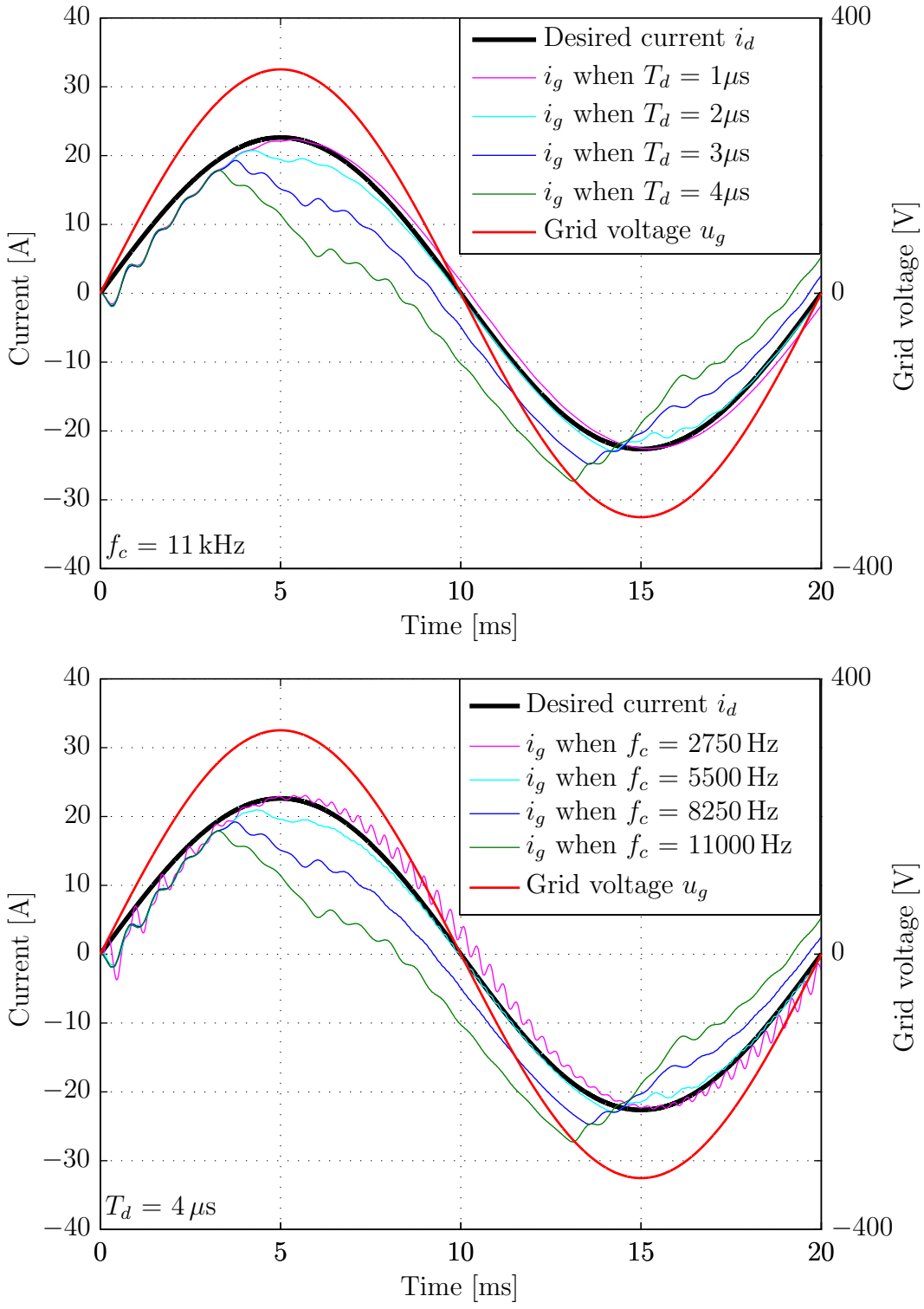


FIGURE 5.19: Simulation of sine current fed into the grid using PWM inverter with dead-time compensator using controllers G_{F1}, G_{F2}, and G_{F3}, for fixed PWM carrier frequency (TOP) and fixed dead time (BOTTOM)

5.3 Testing the PWM Controller

Due to discrepancies between the simulation model and physical inverter hardware, simulations alone cannot be used to verify controller performance. To test the performance of the PWM controller presented in the previous section, the controller and PWM modulator with deadtime compensation were implemented in the Mobile VISMA hardware.

The first concern for the hardware implementation of the controller was whether the feed-forward controller G_{F1} and the voltage compensation controllers G_{F2} and G_{F3} would perform like they did in the simulation model. According to simulation, using voltage compensation controllers G_{F2} and G_{F3} significantly improved the tracking error over using a PI controller alone. The advantage of using the feed-forward controller G_{F1} was not clear.

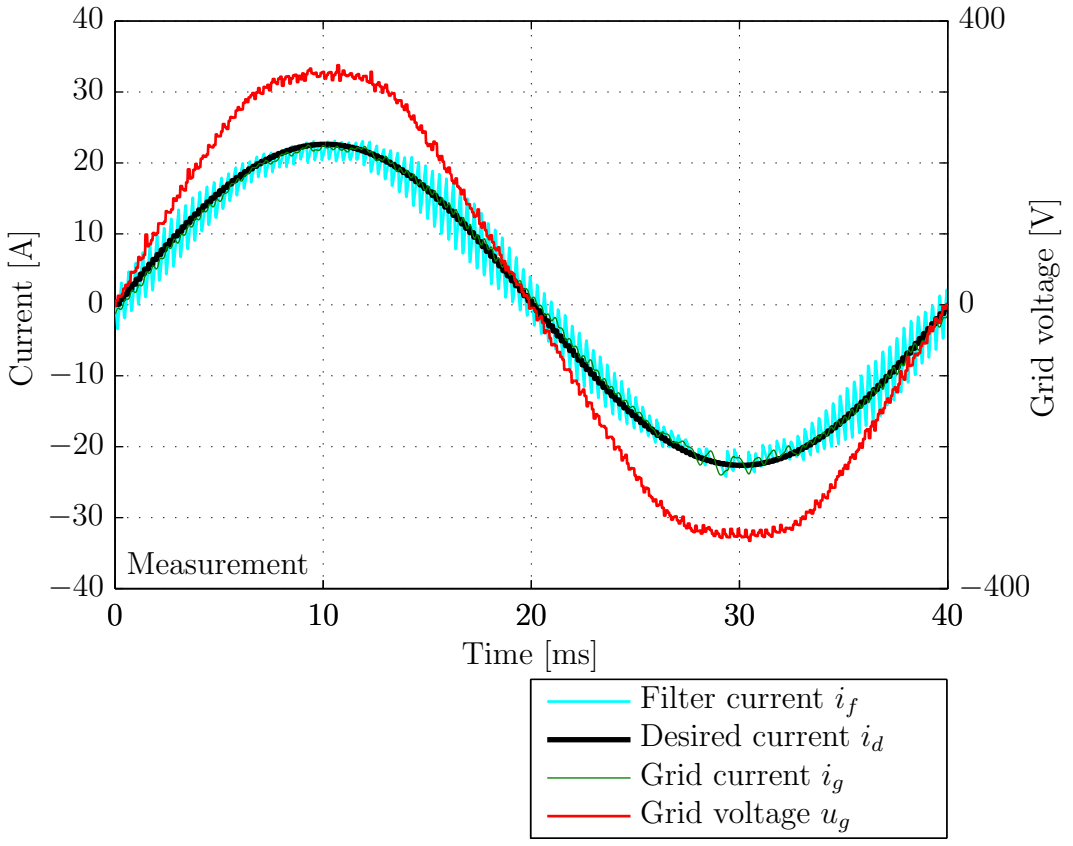


FIGURE 5.20: 16 A current fed into the grid using a PWM controller with voltage compensators G_{F2} and G_{F3} and a feedback PI controller ($K_p = 30\,\mathrm{V/A}$, $K_i = 33000\,\mathrm{V/As}$), PWM carrier frequency $f_c = 5500\,\mathrm{Hz}$

Experiments showed that the grid voltage compensation offered by G_{F2} and G_{F3}, although not as effective as in the simulation, was partially successful and offered an improvement in current tracking performance over the PI controller alone. The feed-forward controller G_{F1}, implemented as a z-transfer function, was found not to improve controller performance and was removed from the control system. Figure 5.20 shows the measurement results for a 16 A sinusoidal current fed into the grid using the PWM controller. One can see that the PWM controller is capable of achieving good current tracking performance (compare to Figure 4.10 on page 49).

A number of parameters influence the performance of the PWM-based current controller. These include the LCL filter parameters, the PWM carrier frequency, PI controller parameters, DC-link battery voltage, and IGBT deadtime. In the following chapter we shall explore how some of these parameters influence the PWM controller performance and compare the performance with that of the hysteresis current controller.

Chapter 6

PWM and Hysteresis Current Controller Performance

In this chapter the performance of the PWM controller is compared to that of the hysteresis current controller for different system configurations. Experimental results are provided which show the step response of the controllers, the performance of the controllers during active and reactive power transfer, and the current harmonics generated by the controllers. Based on the results of these experiments, it can be decided which of the controllers and system configurations are suitable for the Mobile VISMA.

6.1 Variable Parameters

The performance of the controller, whether a PWM controller or a phase current controller is used, depends on the parameters of the controller, inverter, and the grid to which the inverter is connected. The parameters of the system can be divided into three groups: parameters which can be changed in software, parameters which can be changed by modifying the inverter hardware, and parameters over which there is no control.

In the Mobile VISMA, parameters which can be easily modified in software include the proportional and integral gain of the feedback PI controller G_C of the PWM-based controller, the PWM carrier frequency, and the hysteresis limits of the hysteresis current controller. Parameters which can be modified in hardware

with relative ease are the LCL filter parameters. The parameters over which there is no influence include the state and impedance of the grid, as the VISMA is connected to the public grid. Also, the DC-link battery voltage is not stiff and fluctuates depending on the State of Charge (SOC) of the battery and the current being drawn from or fed into the battery. With the NiMH battery pack used in the experimental setup, the DC-link voltage fluctuations can be significant, and the battery voltage can range from $\pm 350\,\mathrm{V}$ to $\pm 400\,\mathrm{V}$.

Because of variations in the properties of the grid and battery voltage, the results of experiments performed on the Mobile VISMA hardware will contain a certain degree of variability. In the experiments performed in this chapter, the conditions of the experiments were kept constant within means, i.e. all experiments were performed with a similar SOC of the battery and within a short period of time. Parameters which could be altered, either in software or with simple hardware modifications, were varied to see which configuration yields best current tracking performance.

In the experiments, the following controllers were tested:

- Hysteresis current controller with $\pm 1\,\mathrm{A}$ hysteresis limits
- PWM current controller with a carrier frequency $f_c = 5.5\,\mathrm{kHz}$ (PI controller parameters: $K_p = 30\,\mathrm{V/A}$, $K_i = 33,000\,\mathrm{V/As}$)
- PWM current controller with a carrier frequency $f_c = 11\,\mathrm{kHz}$ (PI controller parameters: $K_p = 30\,\mathrm{V/A}$, $K_i = 33,000\,\mathrm{V/As}$)

The gain K_p for the PI controller was chosen to be equal to the optimal gain calculated in (5.22), $K_p = 30\,\mathrm{V/A}$. The value of integral components calculated using equation (5.23) was $K_i = 57,775\,\mathrm{V/As}$. This value should be considered the top initial value of K_i for controller commissioning. In the experiments, a smaller integral gain of $K_i = 33,000\,\mathrm{V/As}$ was used, which leads to lower overshoot.

Tests were performed for the following filter configurations:

- $L_{fi} = 3\,\mathrm{mH}$, $C_f = 5\,\mu\mathrm{F}$, $L_{fg} = 1\,\mathrm{mH}$
- $L_{fg} = 3\,\mathrm{mH}$, $C_f = 17\,\mu\mathrm{F}$, $L_{fg} = 1\,\mathrm{mH}$

In all experiments with the PWM-based controller, the grid voltage compensation controllers G_{F2} and G_{F3} were operating in parallel with the feedback controller G_C. In the hysteresis current controller, the voltage compensator G_{F3} was added to compensate for the filter capacitor current.

6.2 Step Response

The desired currents calculated by the VISMA, which are to be fed into the grid by the current controller, will not necessarily be ideal sine waves. Therefore, it is interesting to see how a current controller will behave when feeding non-sinusoidal currents into the grid.

Figure 6.1 shows the results of an experiment, where a current with the form of a step function was fed into the grid using a hysteresis current controller with $\pm 1\,\mathrm{A}$ hysteresis limits (TOP) and a PWM controller with a PWM carrier frequency of $f_c = 5.5\,\mathrm{kHz}$ (BOTTOM). Figure 6.2 shows the result of an identical experiment, only with a higher time resolution.

In the PWM controller, the voltage compensation controllers G_{F2} and G_{F3} as well as the PI feedback controller were enabled. The PI controller parameters were set to $K_p = 30\,\mathrm{V/A}$ and $K_i = 33,000\,\mathrm{V/As}$. The LCL filter configuration used was: $L_{fi} = 3\,\mathrm{mH}$, $L_{fg} = 1\,\mathrm{mH}$, $C_f = 17\,\mu\mathrm{F}$.

The response speeds of the hysteresis controller and PWM controller are comparable. The PWM controller has a slightly longer rise time than the hysteresis controller, but creates less overshoot and has a shorter settling time. In Figure 6.1 one can see that the filter current ripple has a constant amplitude for the hysteresis current controller, but varies with the grid voltage u_g for the PWM current controller. Likewise, in Figure 6.1 one can see how the switching frequency of the hysteresis controller changes with the grid voltage u_g for the hysteresis current controller, but remains fixed for the PWM controller.

In both PWM and hysteresis controllers, the compensator G_{F3} was used, which causes the filter current to have a sinusoidal form, but reduces the waviness of the grid current as the inverter compensates the filter capacitor current.

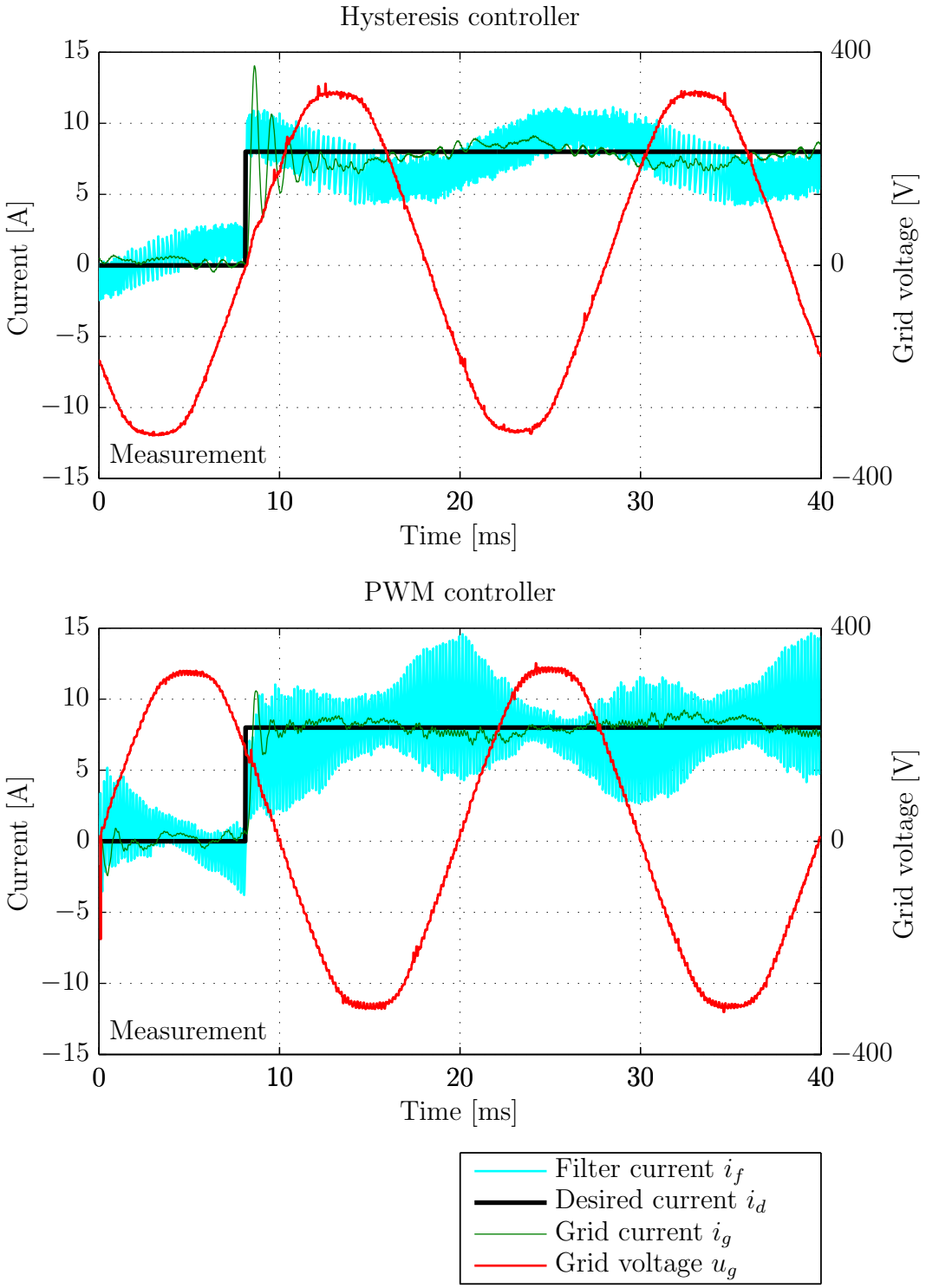


FIGURE 6.1: Step-function currents fed into the grid using a hysteresis current controller with ± 1 A hysteresis limits and compensator G_{F3} (TOP) and a PWM controller with voltage compensators G_{F2} and G_{F3} and a feedback PI controller ($K_p = 30\,\mathrm{V/A}$, $K_i = 33,000\,\mathrm{V/As}$) (BOTTOM).

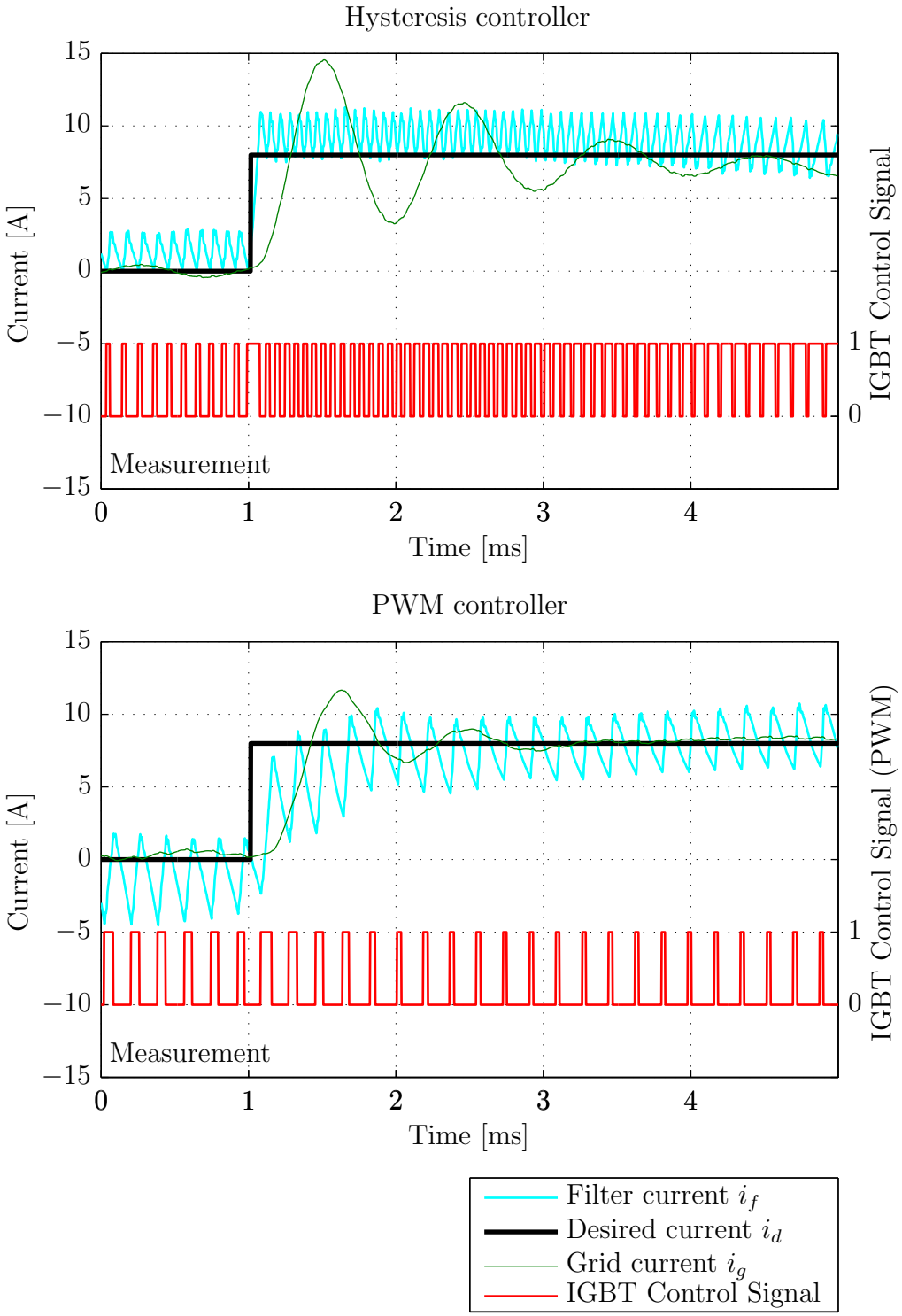


FIGURE 6.2: Step-function currents fed into the grid using a hysteresis current controller with ±1 A hysteresis limits and compensator G_{F3} (TOP) and a PWM controller with voltage compensators G_{F2} and G_{F3} and a feedback PI controller ($K_p = 30\,\mathrm{V/A}$, $K_i = 33,000\,\mathrm{V/As}$) (BOTTOM).

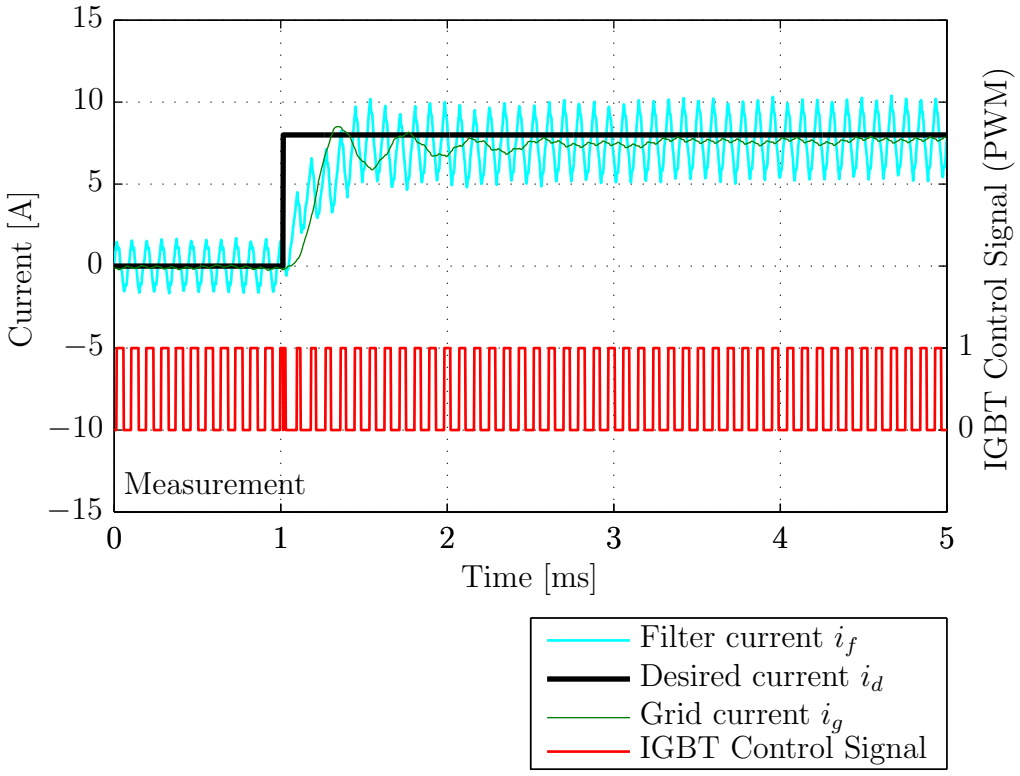


FIGURE 6.3: Step response of PWM controller with carrier frequency $f_c = 11\,\text{kHz}$ and LCL filter configuration: $L_{fi} = 3\,\text{mH}$, $C_f = 5\,\mu\text{F}$, $L_{fg} = 1\,\text{mH}$

Another experiment, the results of which are shown in Figure 6.3, was performed with the PWM controller. In this experiment the PWM carrier frequency was increased to $f_c = 11\,\text{kHz}$ and the filter capacitor size was reduced to $C_f = 5\,\mu\text{F}$. With the higher switching frequency and smaller filter capacitor, the rise time and settling time are shorter. Because of the shorter settling time and less oscillations of the grid current i_g, we can conclude that in terms of the step response, the PWM controller outperforms the hysteresis current controller.

6.3 Active Power Transfers

Figures 6.4 and 6.5 show the results of experiments where active power is drawn and fed into the grid, respectively, using different controllers and LCL filter configurations. The TOP graphs of the figures show the current error $I_e = I_g - I_d$, which is equal to the difference between the actual and desired RMS values of the grid current. The MIDDLE graphs show the THD of the currents, measured with a Fluke 434 Power Analyzer. The bottom graph shows the SSE metric

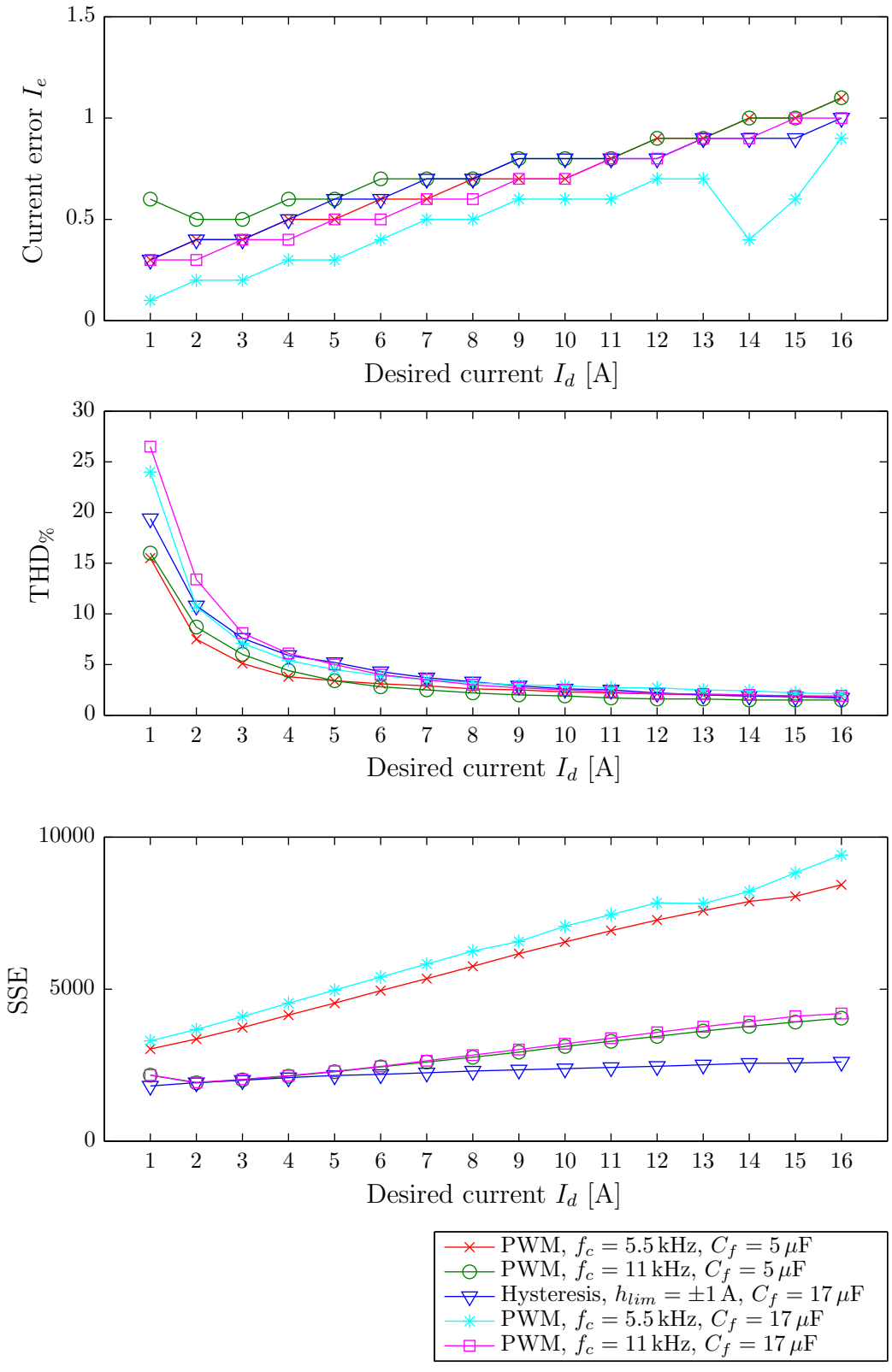


FIGURE 6.4: Battery charging mode current controller performance for different values of the desired RMS current I_d. Error current $I_e = I_g - I_d$ (TOP), THD (MIDDLE), and SSE (BOTTOM) are compared.

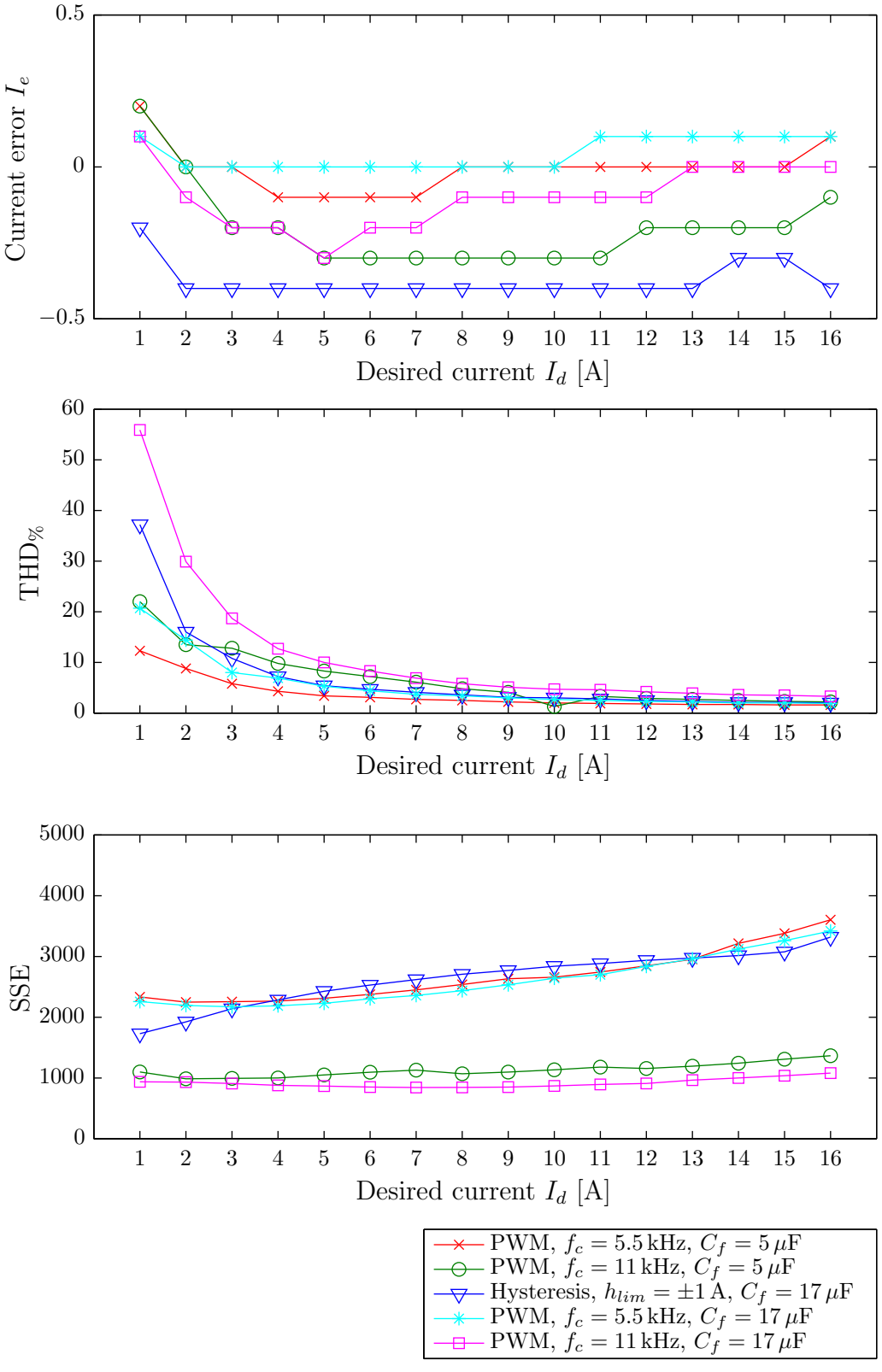


FIGURE 6.5: Feed-in mode current controller performance for different values of the desired RMS current I_d. Error current $I_e = I_g - I_d$ (TOP), THD (MIDDLE), and SSE (BOTTOM) are compared.

used to evaluate current tracking performance, measured with the SSE analyzer implemented in FPGA.

When drawing power from the grid, the grid currents are larger than the desired currents for all system configurations tested, i.e. all controllers draw more power from the grid than intended. When feeding power into the grid, the situation is reversed, i.e. less power is fed into the grid than desired. The current error gets larger for large desired currents. The current errors are similar for all system configurations when charging the battery. When feeding power into the grid, the current errors are largest for the hysteresis controller, and best for PWM controllers with a lower switching frequency (5.5 kHz).

The THD pattern is the same whether power is fed into or drawn from the grid. The THD is high for small currents and low for large currents. The controllers which produce the lowest THD are the PWM controllers when the value of the filter capacitor is small ($C_f = 5\,\mu$F), followed by the hysteresis current controller with a large filter capacitor ($C_f = 17\,\mu$F). It was shown in Figure 6.4 that a hysteresis controller with a small filter capacitor does not perform well when feeding currents into the grid and creates high harmonic distortions, therefore this system configuration is not considered.

In terms of SSE, the hysteresis current controller performs best when drawing power from the grid, followed by PWM controllers with a high PWM carrier frequency ($f_c = 11\,$kHz). When feeding power into the grid, the use of PWM controllers with a high PWM carrier frequency ($f_c = 11\,$kHz) results in the lowest SSE.

Based on these experiments alone, it is difficult to find a winning system configuration, as each configuration has its advantages under different operating conditions.

6.4 Variable Phase Angle

The VISMA may be required to provide or consume reactive power, therefore it is of interest to verify the performance of the current controllers for different phase angles ϕ between the grid current i_g and grid voltage u_g. Experiments were performed where a desired current with an RMS value $I_d = 16\,$A was fed into the grid at different phase angles using different system configurations.

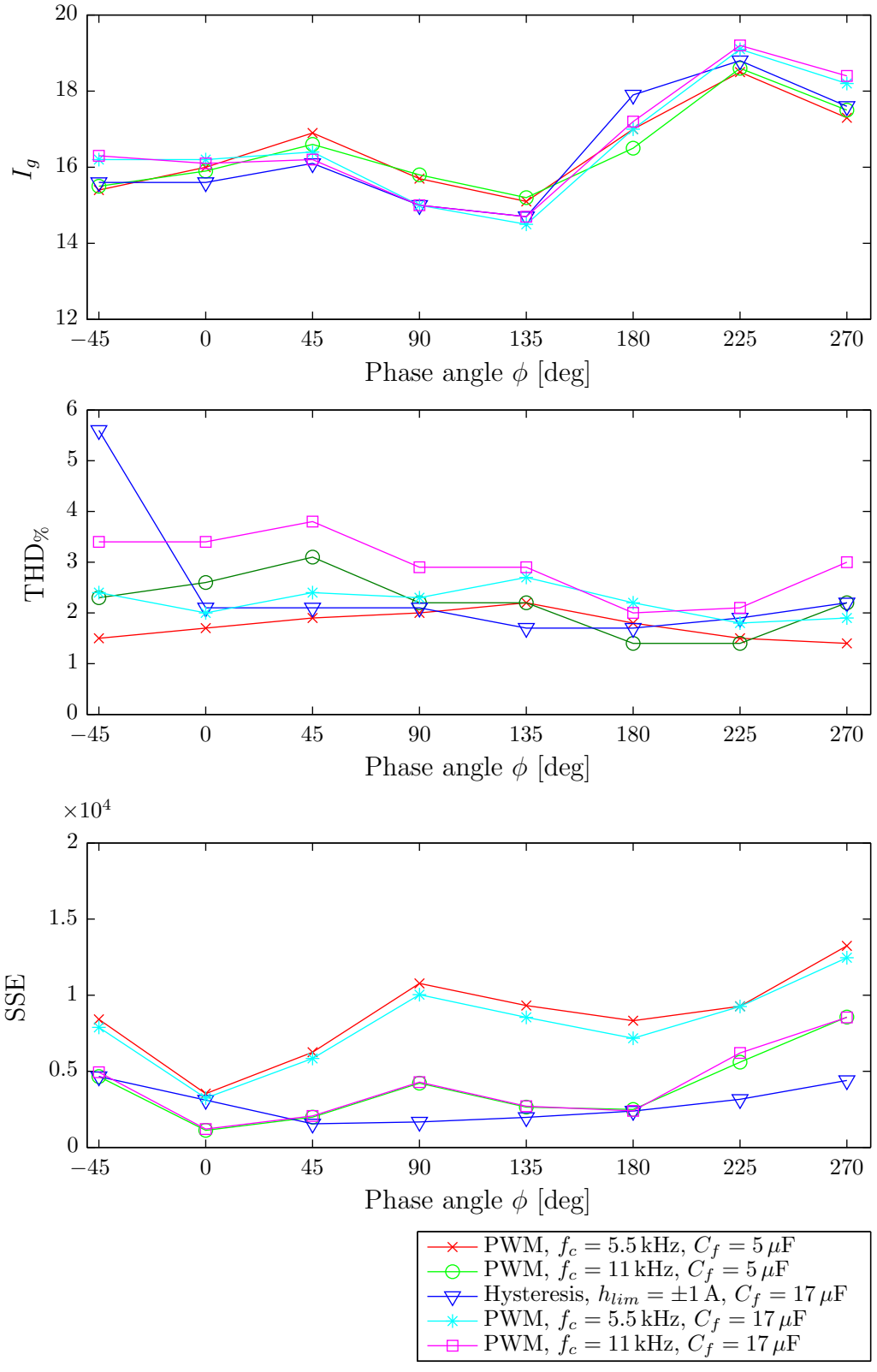


FIGURE 6.6: Comparison of current controller performance for different phase angles for a desired current $I_d = 16\,\text{A}$. I_g (TOP), THD (MIDDLE) and SSE (BOTTOM) are compared.

Type \ Angle		-45	0	45	90	135	180	225	270
Hysteresis	I_g [A]	15.6	15.6	16.1	15.0	14.7	17.9	18.8	17.6
$h_{lim} = \pm 1$ A	THD%	5.6	2.1	2.1	2.1	1.7	1.7	1.9	2.2
$C_f = 17\,\mu$F	SSE	4657	3110	1550	1673	1973	2389	3162	4399
PWM	I_g [A]	15.4	16.0	16.9	15.7	15.1	17.0	18.5	17.3
$f_c = 5.5$ kHz	THD%	1.5	1.7	1.9	2.0	2.2	1.8	1.5	1.4
$C_f = 5\,\mu$F	SSE	8413	3533	6251	10774	9321	8324	9273	13240
PWM	I_g [A]	15.5	15.9	16.6	15.8	15.2	16.5	18.6	17.5
$f_c = 11$ kHz	THD%	2.3	2.6	3.1	2.2	2.2	1.4	1.4	2.2
$C_f = 5\,\mu$F	SSE	4655	1123	1990	4221	2647	2493	5602	8564
PWM	I_g [A]	16.2	16.2	16.4	15.0	14.5	17.0	19.1	18.2
$f_c = 5.5$ kHz	THD%	2.4	2.0	2.4	2.3	2.7	2.2	1.8	1.9
$C_f = 17\,\mu$F	SSE	7887	3240	5844	10037	8545	7170	9260	12462
PWM	I_g [A]	16.3	16.1	16.2	15.0	14.7	17.2	19.2	18.4
$f_c = 11$ kHz	THD	3.4	3.4	3.8	2.9	2.9	2.0	2.1	3.0
$C_f = 17\,\mu$F	SSE	4938	1206	2066	4288	2705	2400	6206	8539

TABLE 6.1: Comparison of the performance of hysteresis and PWM current controllers for different phase angles and different system configurations. A zero phase angle indicates that active power is fed into the grid.

The results of these experiments are presented in Table 6.1 and in Figure 6.6. A zero phase angle $\phi = 0$ indicates that active power is fed into the grid. The current tracking errors are similar for all system configurations. In terms of THD and SEE, each system configuration has its advantages. Overall, the hysteresis current controller performs well, but a high THD was recorded for a phase angle of $\phi = -45°$. The PWM controller with $f_c = 5.5$ kHz and $C_f = 17\,\mu$F has the best overall THD, but has the highest SSE.

Figures 6.7 and 6.8 show the currents and voltages measured in experiments, where the inverter supplies and draws reactive power from the grid, respectively, using a PWM and hysteresis controller.

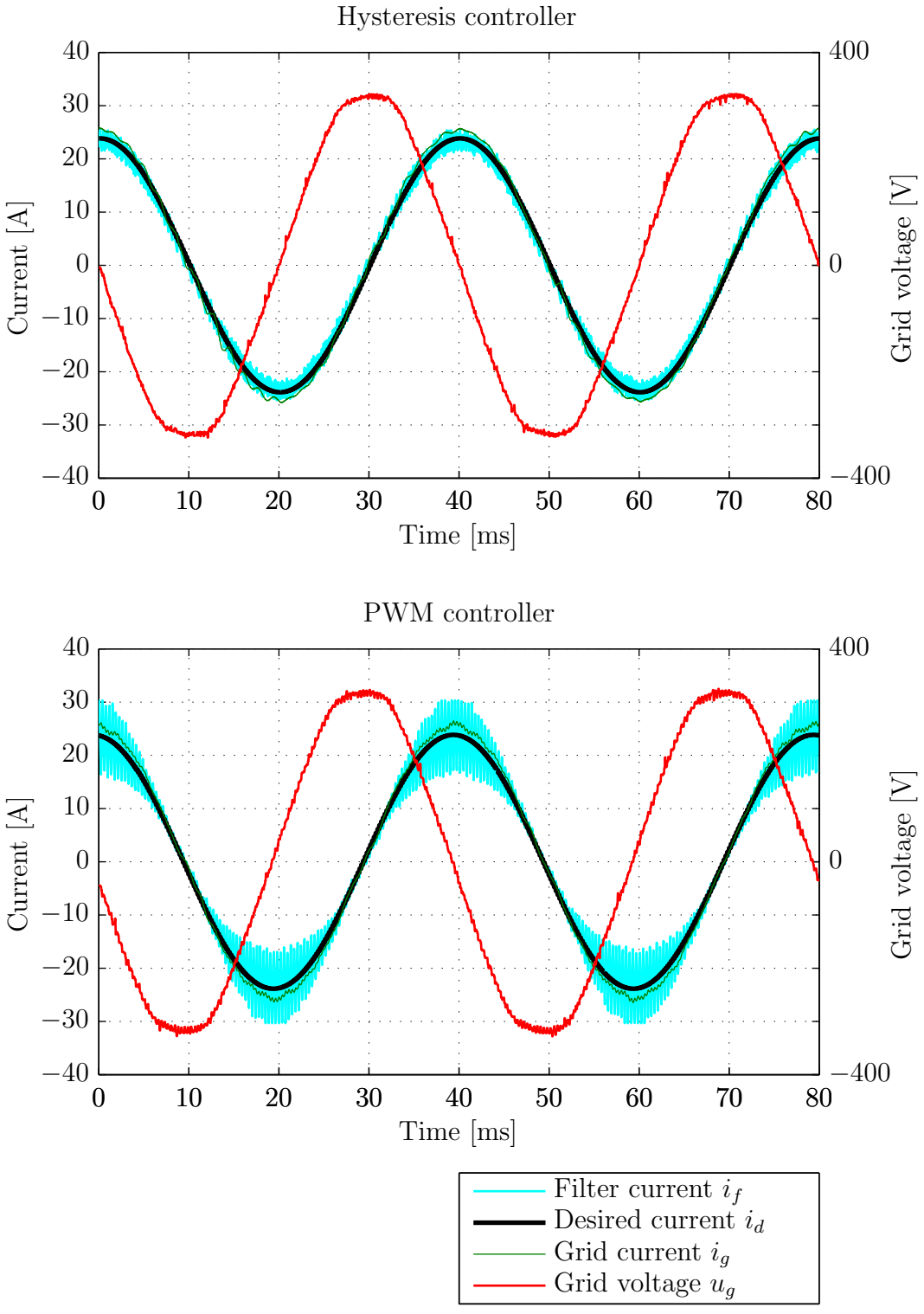


FIGURE 6.7: Currents fed into the grid using hysteresis controller (TOP) and PWM controller (BOTTOM) when voltage leads current by 90° (inductive reactive power is supplied to the grid). LCL filter: $L_{fi} = 3\,\text{mH}$, $L_{fg} = 1\,\text{mH}$, $C_f = 17\,\mu\text{F}$; PWM carrier frequency: $f_c = 5.5\,\text{kHz}$.

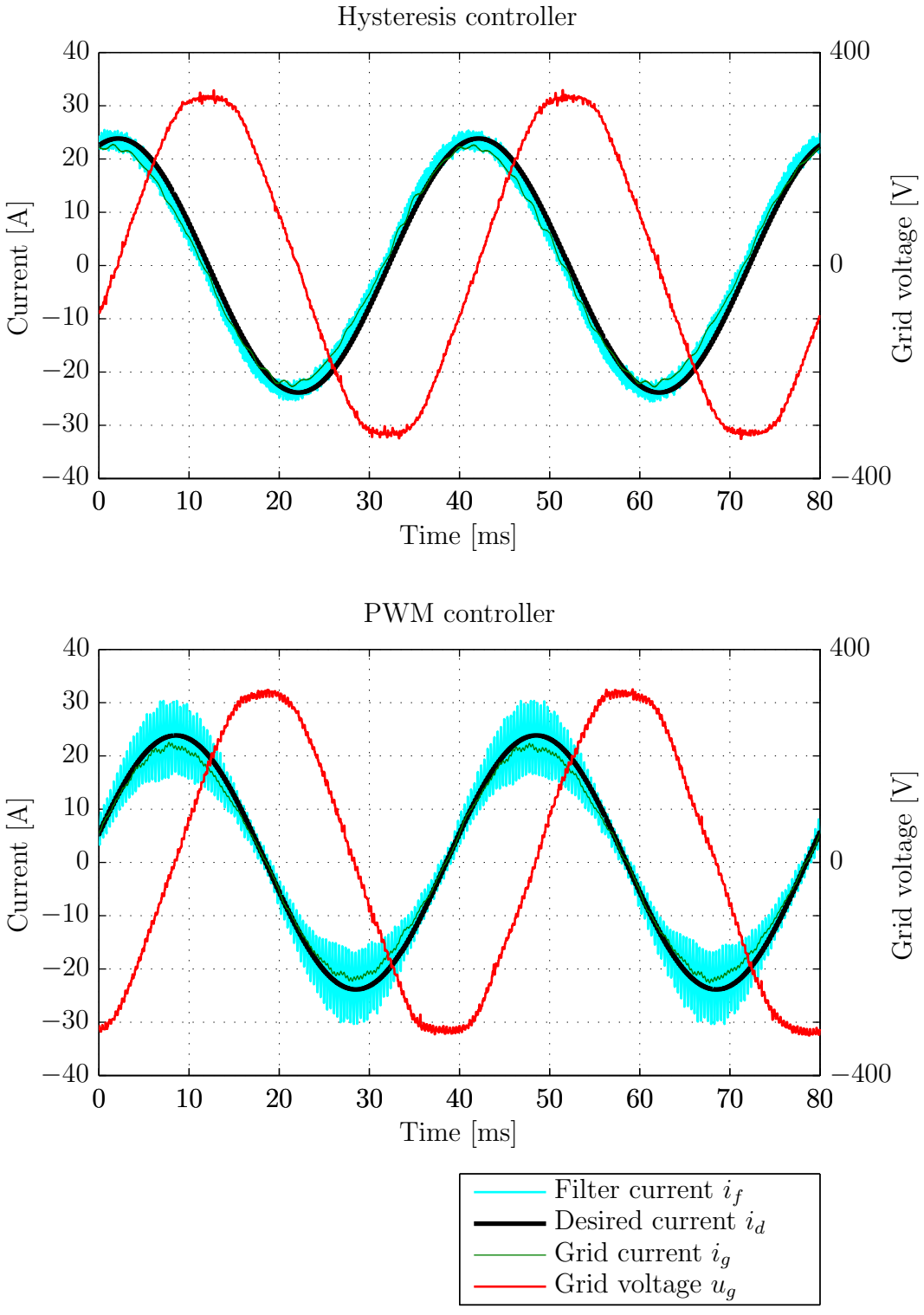


FIGURE 6.8: Currents fed into the grid using hysteresis controller (TOP) and PWM controller (BOTTOM) when voltage lags current by 90° (inductive reactive power is drawn from the grid). LCL filter: $L_{fi} = 3\,\text{mH}$, $L_{fg} = 1\,\text{mH}$, $C_f = 17\,\mu\text{F}$; PWM carrier frequency: $f_c = 5.5\,\text{kHz}$.

6.5 Harmonics

Experiments were performed to measure the individual harmonic currents for different system configurations to help decide which of the controllers and LCL filter parameters produce harmonics which are within the limits set forth by the EN 61000-3-2 standard. The experiments were performed using the Fluke 434 Power Analyzer [45]. The results of these experiments are presented in Figures 6.9-6.12. It was found that, in terms of harmonics, the best performance is achieved by the PWM controller with a PWM carrier frequency $f_c = 5.5\,\text{kHz}$ and an LCL filter configuration with $L_{fi} = 3\,\text{mH}$, $C_f = 5\,\mu\text{F}$, and $L_{fg} = 1\,\text{mH}$ (see Figure 6.9). For this configuration, both in battery charging and grid feed-in modes, the harmonics were below the limits of the EN 61000-3-2 standard. The violation of the hysteresis limits with the other system configurations presented in Figures 6.10-6.12 is small, and with slight tuning of the controller parameters, hardware modifications, or under different grid conditions, the limits of the EN 61000-3-2 standard may be met.

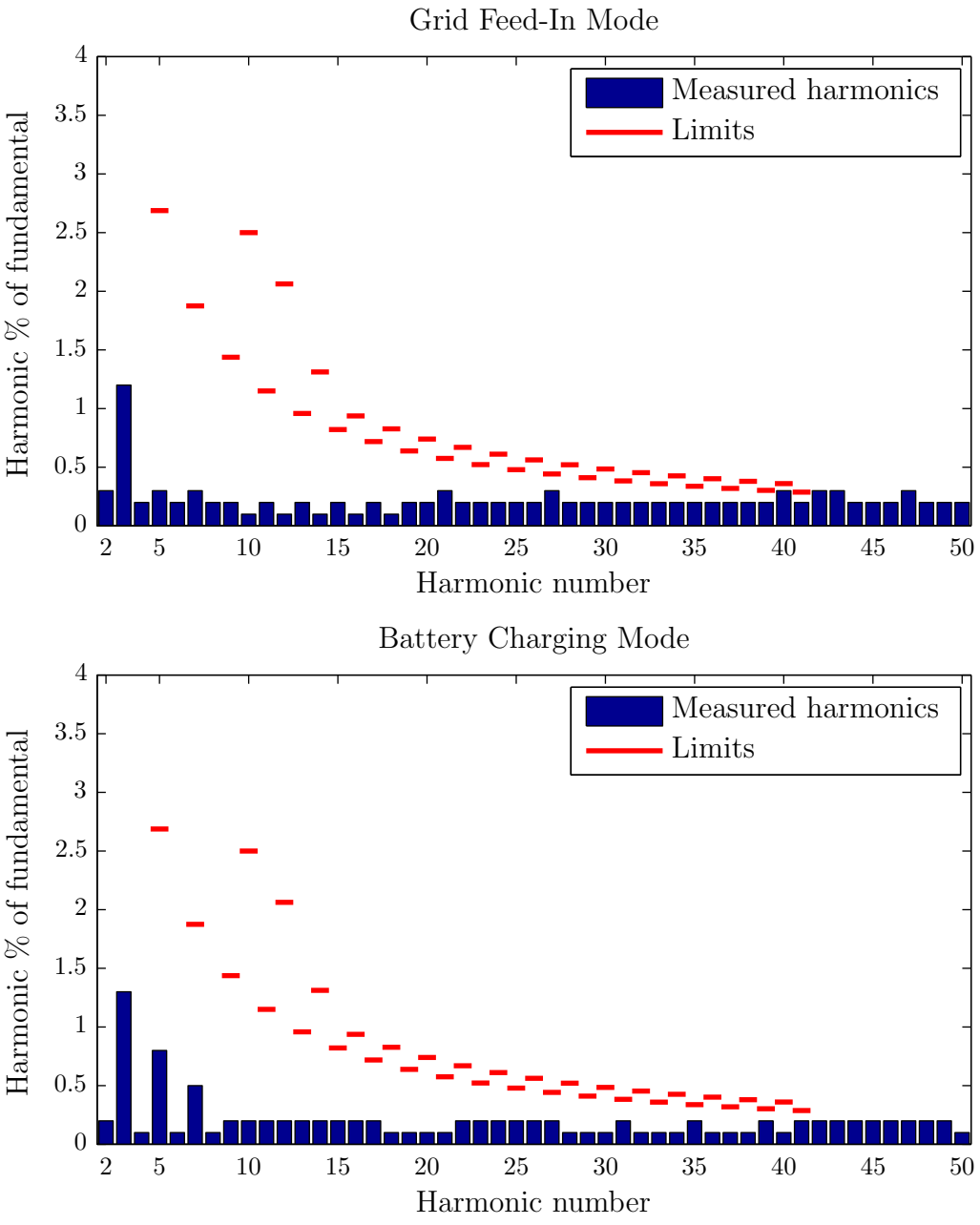


FIGURE 6.9: Harmonics of 16 A current for PWM controller with $f_c = 5.5\,\text{kHz}$ and $C_f = 5\,\mu\text{F}$ and recalculated harmonic limits according to EN 61000-3-2.

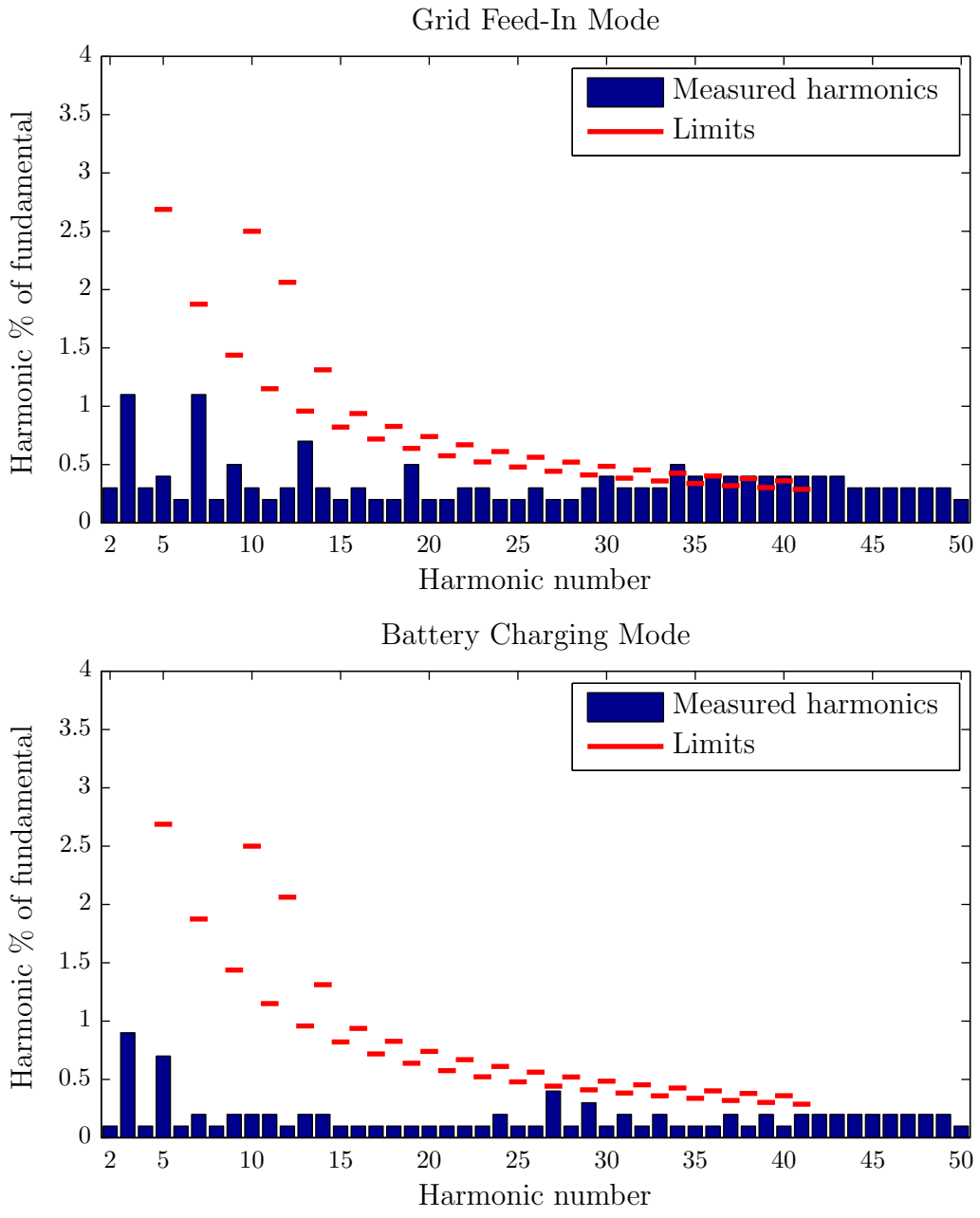


FIGURE 6.10: Harmonics of 16 A current for PWM controller with $f_c = 11\,\text{kHz}$ and $C_f = 5\,\mu\text{F}$ and recalculated harmonic limits according to EN 61000-3-2.

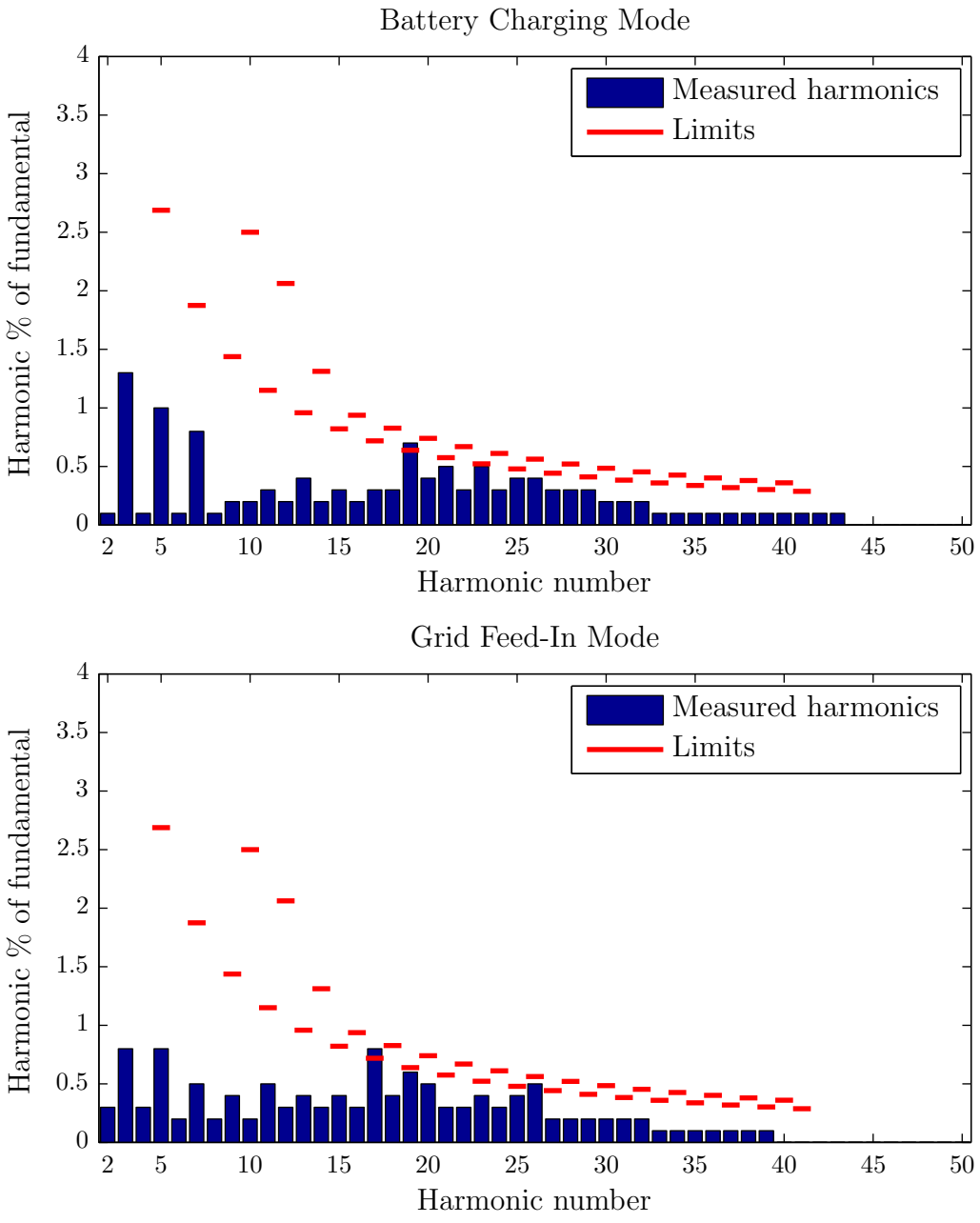


FIGURE 6.11: Harmonics of 16 A current for hysteresis controller with $h_{lim} = \pm 1$ A and $C_f = 17\,\mu$F and recalculated harmonic limits according to EN 61000-3-2.

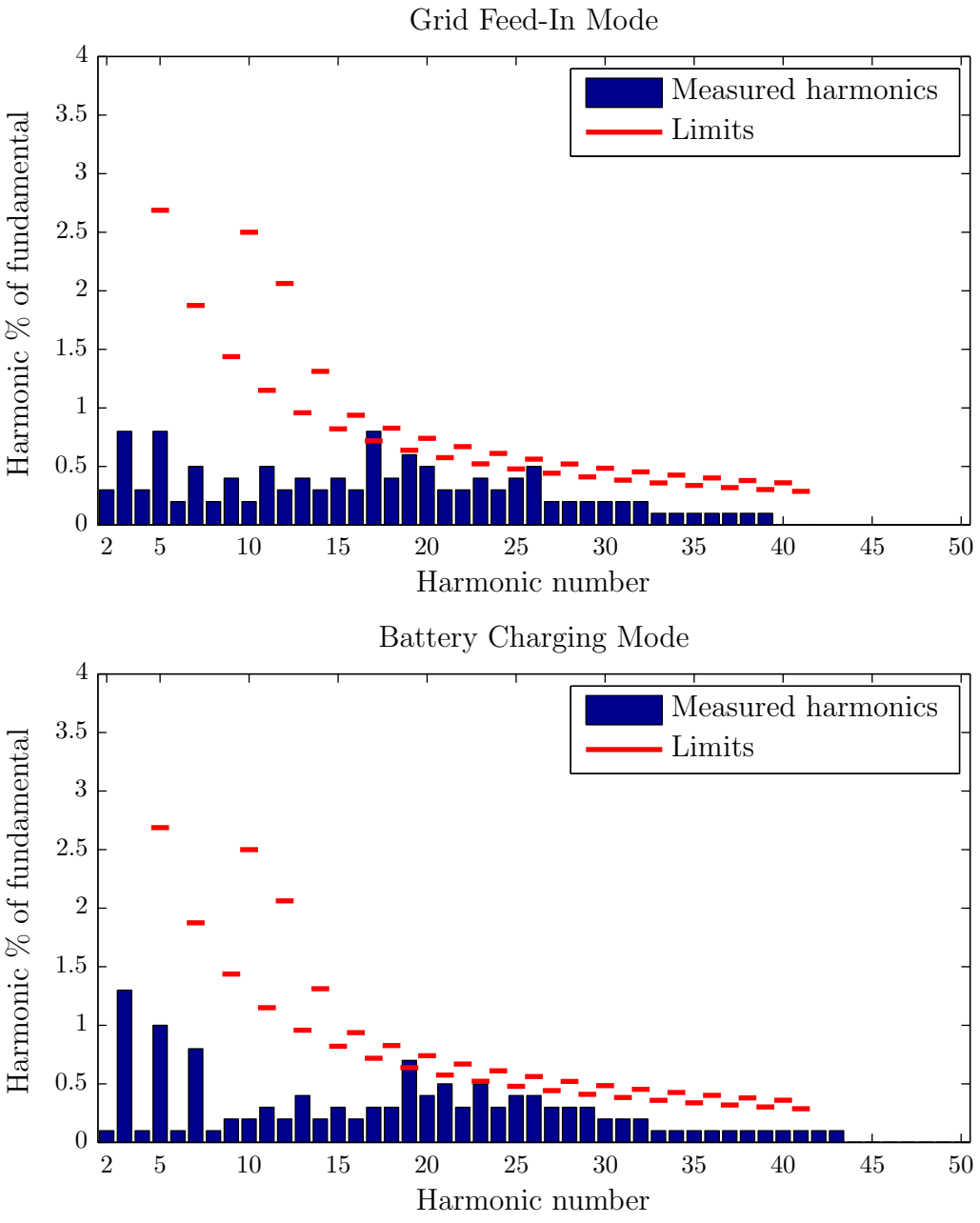


FIGURE 6.12: Harmonics of 16 A current for PWM controller with $f_c = 5.5\,\text{kHz}$ and $C_f = 17\,\mu\text{F}$ and recalculated harmonic limits according to EN 61000-3-2.

6.6 Summary

In terms of the step response, the PWM controller performs best due to its low overshoot and fast settling time. During active and reactive power transfers, each of the controllers and configurations had its advantages under certain operating conditions. In terms of harmonics, a PWM controller performed best and met the requirements of the EN 61000-3-2 standard; however, the violation of harmonic limits created by the hysteresis current controller was not large and can likely be averted by tuning the LCL filter parameters, hysteresis limits, and using faster IGBTs with a shorter deadtime. The major advantage of the PWM current controller is that it has a fixed switching frequency; therefore, the LCL filter can be designed in such a way that the resonance will not be excited. Furthermore, the PWM controller was found to operate well with a smaller filter capacitor. In case of the hysteresis current controller, a large filter capacitor needs to be used to ensure stability. The problem with using a large filter capacitor is that the capacitor current has to be compensated for by the inverter, and, in case of a short circuit or grid disturbance, the current between the capacitor and the grid cannot be controlled.

The hysteresis current controller is simpler to implement than the PWM controller. For the hysteresis current controller, only the filter currents need to be measured, whereas for the PWM current controller, the grid voltage must also be measured and used as an input to the grid-voltage compensator, without which the PWM controller performs poorly. Since the grid voltage measurement is already needed for the VISMA, this does not pose a problem. The effectiveness of the voltage compensator depends on how well the inverter can feed in the desired voltage into the grid; therefore, deadtime compensation should be used in the PWM inverter.

Based on the experiments performed in this chapter, it can be concluded that both the hysteresis controller and the PWM controller can be used for the VISMA. In case of the hysteresis current controller, it would be of advantage to use faster IGBTs with a shorter deadtime, in which case the hysteresis limit violations would be reduced, improving current tracking performance and reducing the harmonic distortion.

Chapter 7

Faults in the Power Network

In this chapter the standards regarding the behavior of distributed generators in case of power network faults are discussed, and the fault ride-through requirements for the VISMA inverter are defined. The fault ride-through characteristics of a VISMA are compared to those of an electro-mechanical synchronous machine. Next, short-circuit experiments on the Mobile VISMA are presented to show that the inverter is capable of fault ride-through, and further experiments are shown which explain the behavior of the VISMA during power network faults. Finally, a procedure for reconnecting the VISMA to the grid after a long-lasting power network fault is presented.

7.1 Power System Faults and Protective Systems

A fault in an electrical power system is the unintentional and undesired creation of a short circuit or open circuit [54]. Short circuit faults are most common, and they can be categorized into one of the following four types: single line-to-ground, line-to-line, double line-to-ground, and balanced three phase. The most common form of short circuits results from insulator flashover during electrical storms creating single-phase faults, whereas other causes of short circuits can include power line damage by wind, falling trees, excessive ice loading, etc. [55]. In a short-circuit fault, high currents flow through the electrical network towards the fault point, causing large voltage drops in parts of the grid close to the fault, and in case of non-symmetrical faults, unbalanced operating conditions. If the fault is not

promptly isolated, the high current can lead to overheating and damage of network components.

The power network is equipped with protective systems which isolate faulty parts from the rest of the network. A number of technologies can be used to detect and isolate network faults. Fuses and circuit breakers react to the overcurrents caused by a fault, disconnecting the circuit. A fuse disconnects the circuit if the current that passes through it exceeds the fuse rating for a time long enough for the I^2R losses to heat and melt the fuse linkage. Like fuses, circuit breakers are protective elements which respond to an overcurrent, disconnecting the circuit, and are available in both magnetic and thermal designs [56]. Relays combined with fault-detecting units based on principles other than overcurrent protection are available; however, in modern electrical power networks, overcurrent fault protection devices play a dominant role. In the traditional centralized power network, large synchronous generators delivered the short-circuit current necessary to actuate the fault protection systems. A short-circuited synchronous machine automatically reacts to the short circuit, delivering a fault current much higher than its nominal current. Distributed generators which are connected to the power network through grid-tie inverters do not exhibit the same behavior.

7.2 Standards Governing Fault Behavior of Distributed Generators

In Germany, different standards describing the specifications of generation facilities connected to the power grid apply to generation facilities depending on their output power and the voltage level they operate on. For distributed generators with more than 100 kW peak power operating on the medium-voltage level, the Guideline for the Connection and Parallel Operation of Generation Facilities in the Medium Voltage Network (*Richtlinie für Anschluss und Parallelbetrieb von Erzeugungsanlagen am Mittelspannungsnetz*) [57], to which we will from now on refer to as the medium voltage guideline, was established in 2008 by BDEW, the German Association of Water and Energy Industries (*Bundesverband der Energie- und Wasserwirtschaft*). This guideline requires generation facilities working on the medium voltage level to dynamically support the network, i.e. the generation devices should technically be able not to disconnect from the grid during faults,

support the voltage in the grid by supplying a reactive current, and not draw more inductive reactive power from the grid after detecting a fault than before the fault [57]. The required fault ride through duration without disconnection from the grid can range from 150 ms to 1500 ms and depends on the measured grid voltage during the fault and the type of generating device as defined by TransmissionCode 2007 [58], a document describing the network and system rules for German transmission network operators. According to the BDEW guideline, the issue whether to provide a short circuit current during the fault ride through should be discussed with the network operator.

For small generators operating on the low-voltage network, as of 2011, no standards existed requiring fault ride through. In August 2011, the application guide VDE-AR-N 4105 [42] was published by the Association of Electrical Engineering, Electronics, and Information Technology (*Verband der Elektrotechnik Elektronik Informationstechnik e.V.*) (VDE) describing the minimum technical requirements for the connection and parallel operation of generation facilities on the low-voltage power network (see Appendix C.2). According to this guide, polyphase, inverter-coupled generation facilities must have the technical capabilities of polyphase synchronous generators. The guide also specifies that generation facilities on low-voltage networks should participate in static voltage stabilization, but no dynamic voltage stabilization is required. VDE-AR-N 4105 does not set any requirements for fault ride through for this class of devices and orders the disconnection of the devices from the grid if the voltage drops below 80% of the nominal voltage within 200 ms using a progammable protection relay.

Even though the Mobile VISMA operates on the low-voltage network and is a low power device, the idea of the VISMA is to support the power network like an electromechanical synchronous machine operating on the middle voltage level. Therefore, the middle voltage guideline was used as a specification reference to define the desired response of the VISMA to grid faults.

7.3 Grid-Tie Inverter Behavior During Power System Faults

The grid-tie inverter of the VISMA must be resistant to power system faults and capable of fault ride through. Based on this, we can define three requirements

that the inverter and current controller should fulfill:

- The inverter power electronics may not be damaged as a result of a power system fault.
- A power system fault should not cause the internal protection systems of the inverter (e.g. fuses or circuit breakers) to trip.
- The inverter should be able to feed the desired current (not exceeding the inverter current rating) into the grid during a fault.

At this point, it is important to discuss the difference between the current ratings of an electromechanical generator and a grid-tie inverter. A synchronous generator operating at its full rated power feeding energy into the grid, when short circuited, will for a short time provide a large short circuit current, which can be approximately eight times higher than the current before the fault, without sustaining damage to the synchronous machine. The short circuit power of the machine, defined as the product of the short circuit current and the nominal voltage, $S_{ss} = I_{ss}, \cdot U_n$, is much higher than the nominal power. The machine windings, being constructed of copper wire, can withstand short lasting overcurrents due to their thermal capacity. The situation is different for semiconductor-based grid-tie inverters. An overcurrent in the semiconductor switch can quickly lead to an overheating at the junction and thus to a device breakdown. For illustration purposes, let us consider the Fuji IGBT IPM used in the Mobile VISMA inverter. In the datasheet [33] we can find that the absolute maximum continuous collector current rating is 50 A whereas the peak current rating is 100 A for 1 ms. A higher or longer lasting current will cause heat buildup at the junction, which cannot be dissipated quickly enough, causing device failure.

Unlike an electromechanical synchronous machine, a grid-tie inverter operating at its full rated power feeding energy into the grid, when short circuited, cannot respond to the fault with a higher current. The short circuit current is limited to the maximum current the inverter is designed for. A grid-tie inverter is designed to work with currents within the operating range of the semiconductor switching devices it uses, and the current controller input range as well as the sensors used for current feedback are scaled to work within this range. This has consequences for the VISMA. During a network fault, the VISMA cannot provide currents larger than what the inverter is designed for. If from the machine model a desired current

is calculated that exceeds the inverter limits, clipping must be implemented to prevent an overcurrent situation and damage to the inverter.

It is possible to design an inverter with a peak current rating higher than its continuous current rating. For this, the thermal layout of the inverter components can be made for the continuous current rating, whereas the semiconductor switching devices should be chosen to support the peak current. Also, the filter inductors should be chosen not to enter saturation at the peak current, and the current sensors should be used that can handle peak current values.

7.4 Short-Circuit Tests of the Grid-Tie Inverter

Short-circuit tests were designed to check the inverter performance during network faults and to determine whether the inverter and current controller can meet the fault ride through requirements specified in Section 7.3. The tests have been divided into two categories, off-grid and online tests. In the off-grid tests, the inverter is short-circuited directly at its output terminals and operated without a connection to the grid or any load, and it feeds a sinusoidal current of given frequency and amplitude into the short circuit. Using this configuration, the short-circuit performance of the controller can be verified. In the online tests, the inverter is connected and operates in parallel to the grid, feeding in currents calculated using the VISMA algorithm. An external device is used to generate grid faults, allowing the observation of the VISMA's response to the faults.

7.4.1 Off-grid short-circuit tests

Two scenarios for off-grid short-circuit tests are presented in Figures 7.1 and 7.2, which depict a 3-phase balanced phase-to-phase short circuit and a balanced phase-to-neutral short circuit, respectively. The scenarios are realized by physically short-circuiting the outputs of the inverter and using the inverter to supply a 3-phase symmetrical sinusoidal current to the short circuit. The current can be varied up to the maximum current rating of the inverter, which is 16A RMS. The inverter is supplied by a DC-link voltage of $\pm U_{DC}$ and has an output LCL filter on each phase comprising inductors L_{fi} and L_{fg} and a capacitor C_f. A NiMH battery pack charged to a voltage of approximately $\pm 380\,V$ is used to supply the DC link

voltage in the experiments. The objective of the off-grid tests can be summarized as follows:

- Verify if the inverter can provide a short-circuit current equal to the maximum current rating of the inverter
- Compare the hysteresis current controller to the PWM controller

In the experiments, a hysteresis current controller with ±1A hysteresis limits was compared to a PWM controller with a carrier frequency of $f_c = 11\,\text{kHz}$. The LCL filter configuration was $L_{fi} = 3\,\text{mH}$, $L_{fg} = 1\,\text{mH}$, and $C_f = 17\,\mu\text{F}$ for the hysteresis current controller and $L_{fi} = 3\,\text{mH}$, $L_{fg} = 1\,\text{mH}$, and $C_f = 5\,\mu\text{F}$ for the PWM controller.

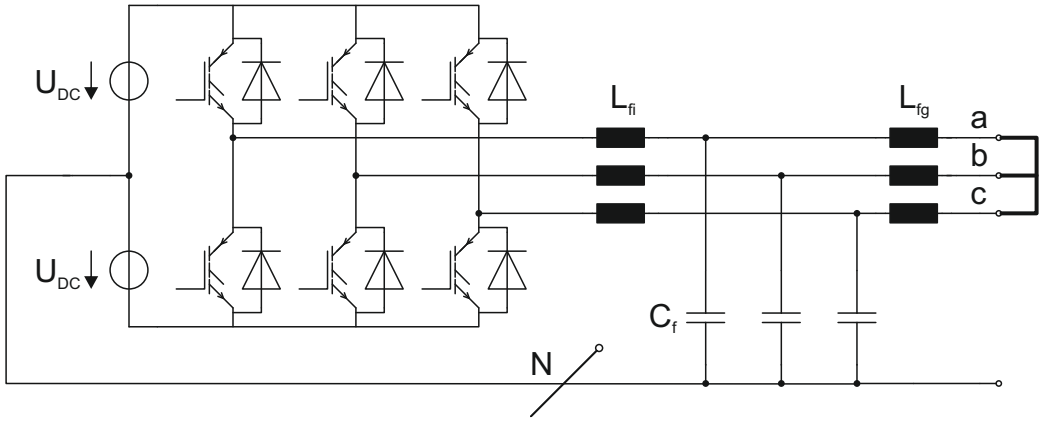


FIGURE 7.1: 3-phase balanced phase-to-phase short circuit

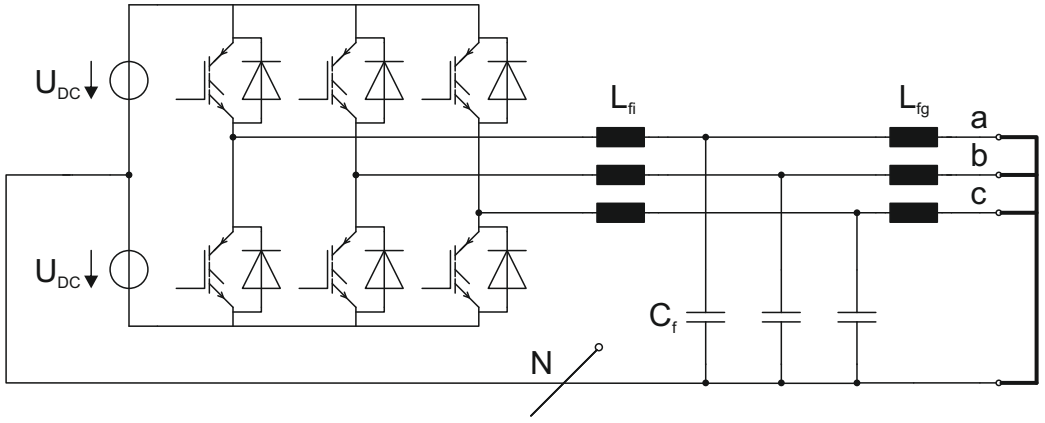


FIGURE 7.2: 3-phase balanced phase-to-neutral short circuit

7.4.1.1 3-phase balanced phase-to-phase short circuit

Figures 7.3 and 7.4 show the measured phase currents fed into the short circuit using the hysteresis and PWM controllers, respectively. Harmonic analysis can be used to determine which of the two currents is of better quality, as this is not evident from the figures.

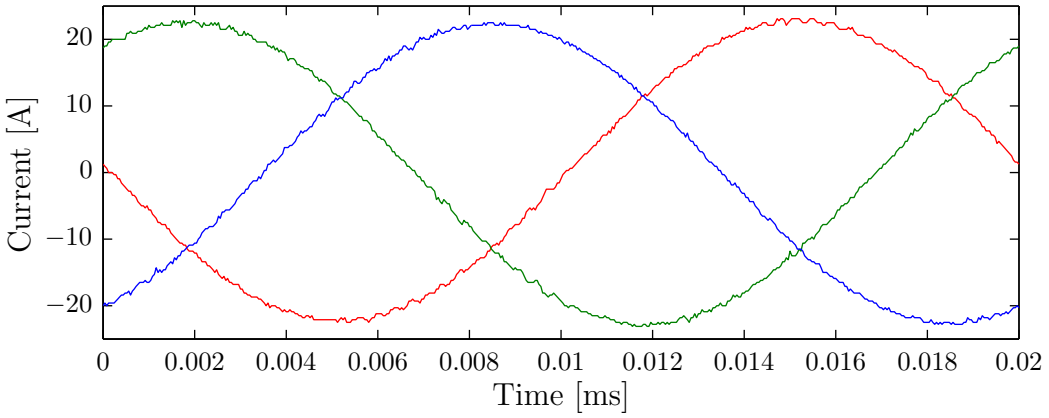


FIGURE 7.3: 3-phase balanced phase-to-phase short-circuit currents fed in using hysteresis current controller with ±1 A hysteresis limits

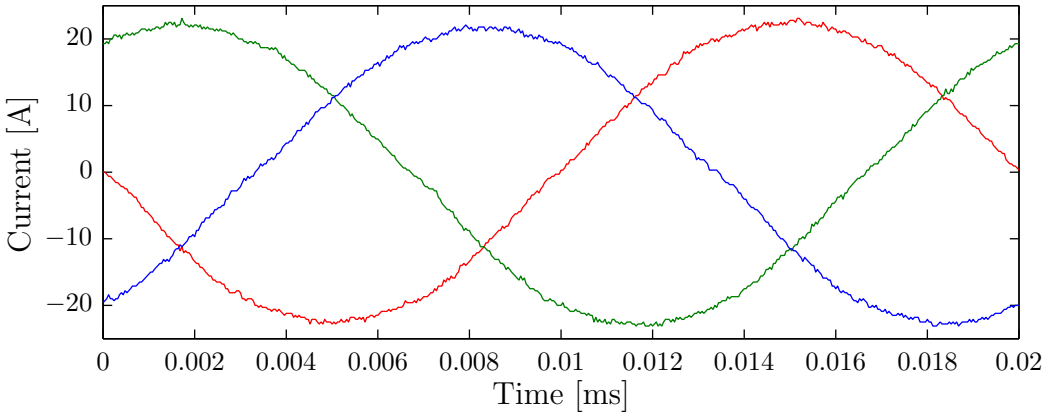


FIGURE 7.4: 3-phase balanced phase-to-phase short-circuit currents fed in using PWM-based controller with 11 kHz carrier frequency

Figures 7.5 and 7.6 show histograms of the switching frequencies of the hysteresis and PWM controllers, respectively, when delivering the 16 A RMS short-circuit current. The hysteresis current controller has switching frequencies ranging from 7,500 Hz to 15,000 Hz. The carrier frequency for the PWM controller is 11 kHz;

however, the histogram shows that a small proportion (less than 4%) of the switching frequencies are different from the PWM carrier frequency. This can be attributed to the fact that, occasionally, the desired voltage u_d and PWM carrier signal may intersect more than twice or less than twice during one period of the carrier signal, creating PWM switching frequencies different than the carrier frequency.

If we consider the harmonics of the short circuit current, we find that the hysteresis current controller outperforms the PWM-based controller. This may be due to the higher average switching frequency achieved by the hysteresis controller. The THD of the short circuit currents is 0.8% and 2.7% for the hysteresis and PWM controllers, respectively. Figure 7.7 and Figure 7.8 show the harmonic analyses of the short circuit currents for a single phase for the hysteresis and PWM controllers, respectively, as well as the harmonic limits according to the EN 61000-3-2 standard for a 16 A current. Both the hysteresis and PWM controller can provide short-circuit currents within the harmonic limits.

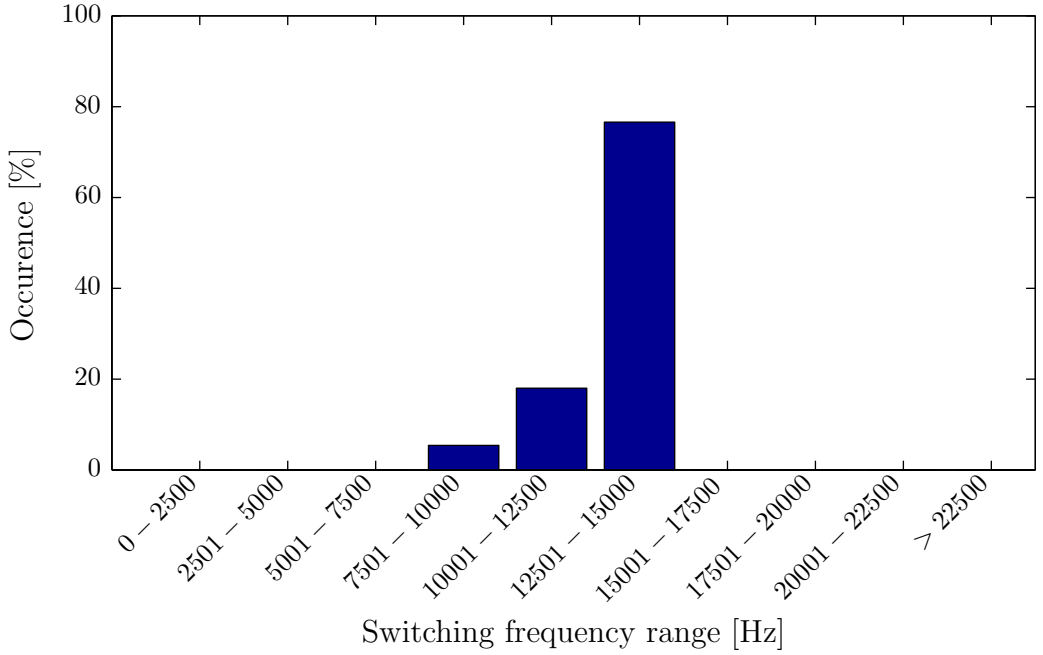


FIGURE 7.5: Switching frequency histogram for hysteresis controller delivering phase-to-phase short circuit current.

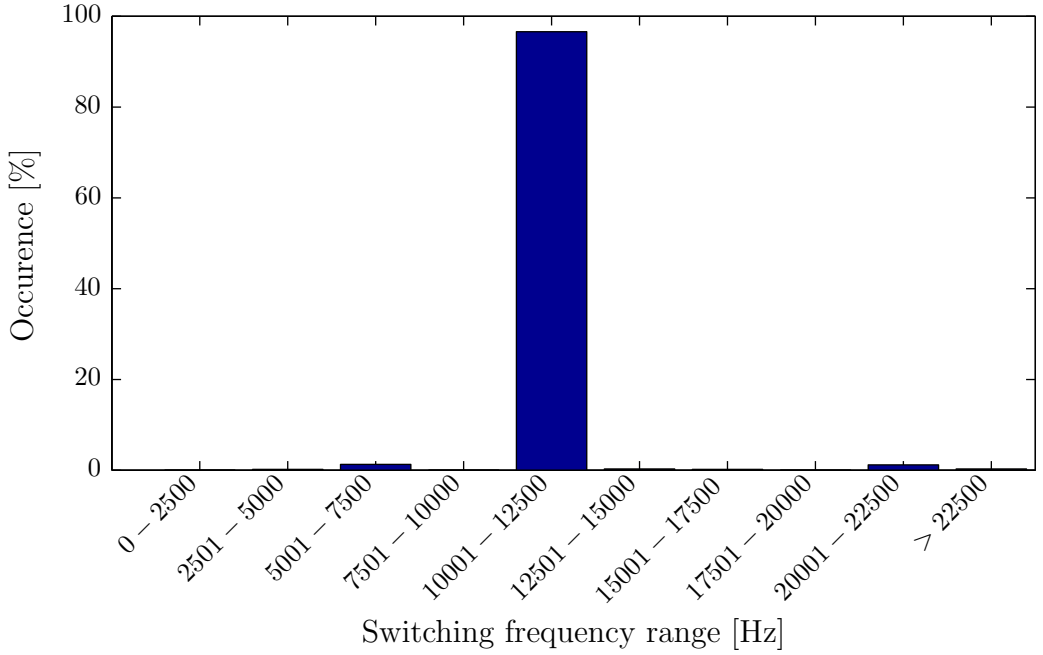


FIGURE 7.6: Switching frequency histogram for PWM controller delivering phase-to-phase short circuit current. The PWM carrier frequency is $f_c = 11\,\mathrm{kHz}$.

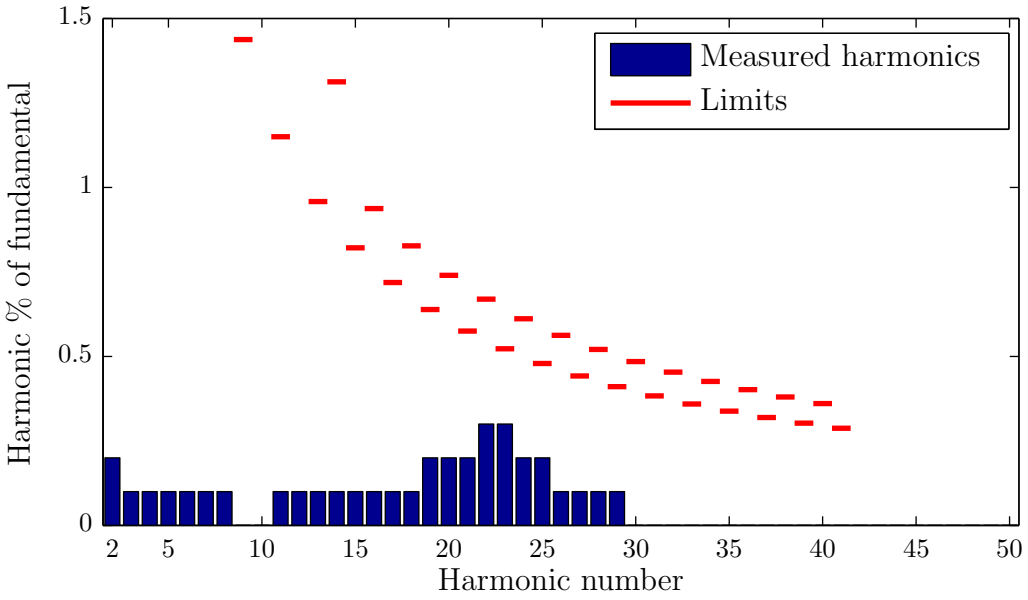


FIGURE 7.7: Harmonics of 16 A phase-to-phase short-circuit current for hysteresis controller with $h_{lim} = \pm 1$ A and $C_f = 17\,\mu$F, and recalculated harmonic limits according to EN 61000-3-2. The shown harmonics, measured using a Fluke 734 power analyzer, are expressed as a percent of the fundamental (50 Hz). The measured THD is 0.8%.

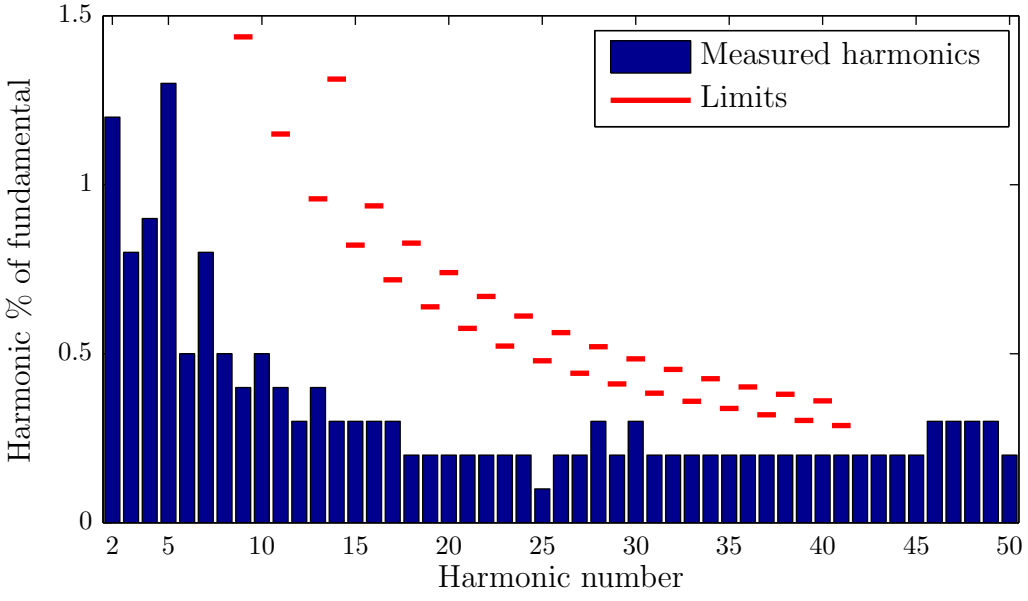


FIGURE 7.8: Harmonics of 16 A phase-to-phase short-circuit current for PWM controller with $f_c = 11$ kHz and $C_f = 5\,\mu$F, and recalculated harmonic limits according to EN 61000-3-2. The shown harmonics, measured using a Fluke 734 power analyzer, are expressed as a percent of the fundamental (50 Hz). The measured THD is 2.7%.

7.4.1.2 3-phase balanced phase-to-neutral short circuit

The performed phase-to-neutral short-circuit experiments were identical to the ones performed for the phase-to-phase short circuit, except that the outputs of the inverter were short-circuited to the neutral as shown in Figure 7.2.

As in the case of the phase-to-phase short circuit, for the phase-to-neutral short circuit, both the hysteresis controller and the PWM controller are capable of delivering a short-circuit current as high as the maximum inverter current rating of 16 A RMS, giving the inverter a short-circuit power of 11 kW.

The THD of the short circuit currents is 0.7% and 1.1% for the hysteresis and PWM controllers, respectively. Figure 7.7 and Figure 7.8 show the harmonic analyses of the phase-to-neutral short-circuit current for a single inverter phase for the hysteresis and PWM controllers, respectively, as well as the harmonic limits according to the EN 61000-3-2 standard for a 16 A current. The harmonics of the short-circuit currents are larger for the PWM controller than for the hysteresis controller, but both controllers can provide short-circuit currents within the harmonic limits.

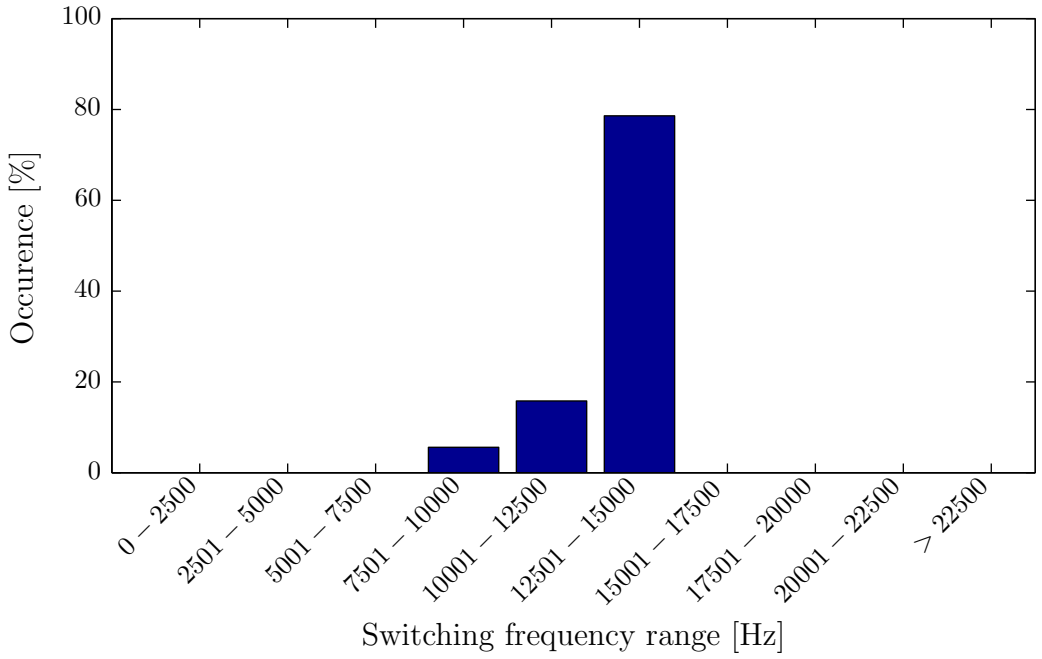


FIGURE 7.9: Switching frequency histogram for hysteresis controller delivering phase-to-neutral short circuit current.

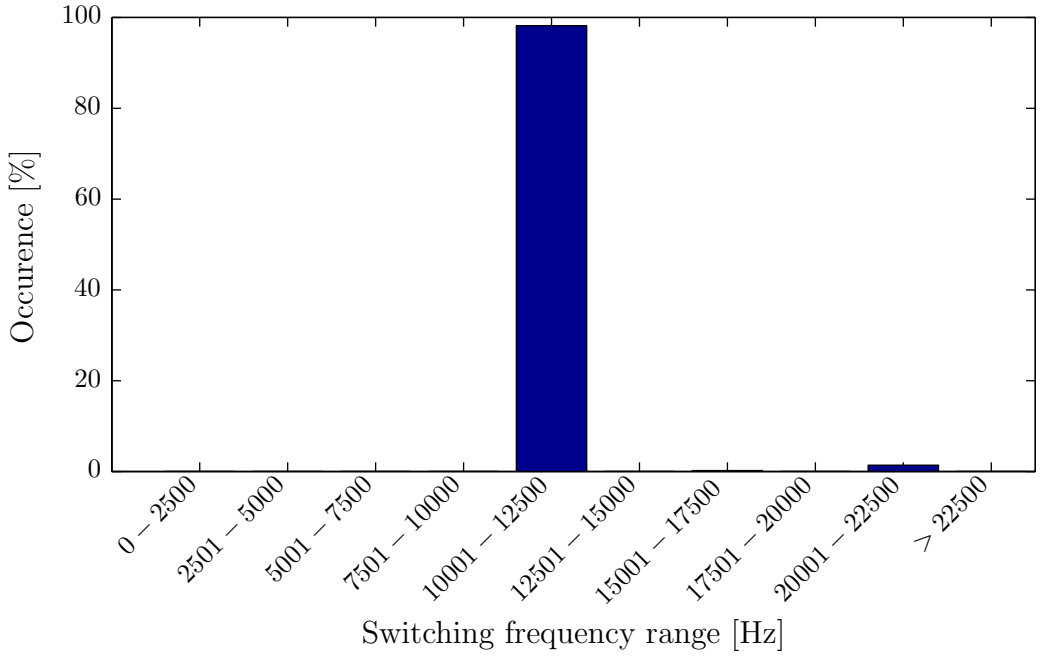


FIGURE 7.10: Switching frequency histogram for PWM controller delivering phase-to-neutral short circuit current. The PWM carrier frequency is $f_c = 11\,\text{kHz}$.

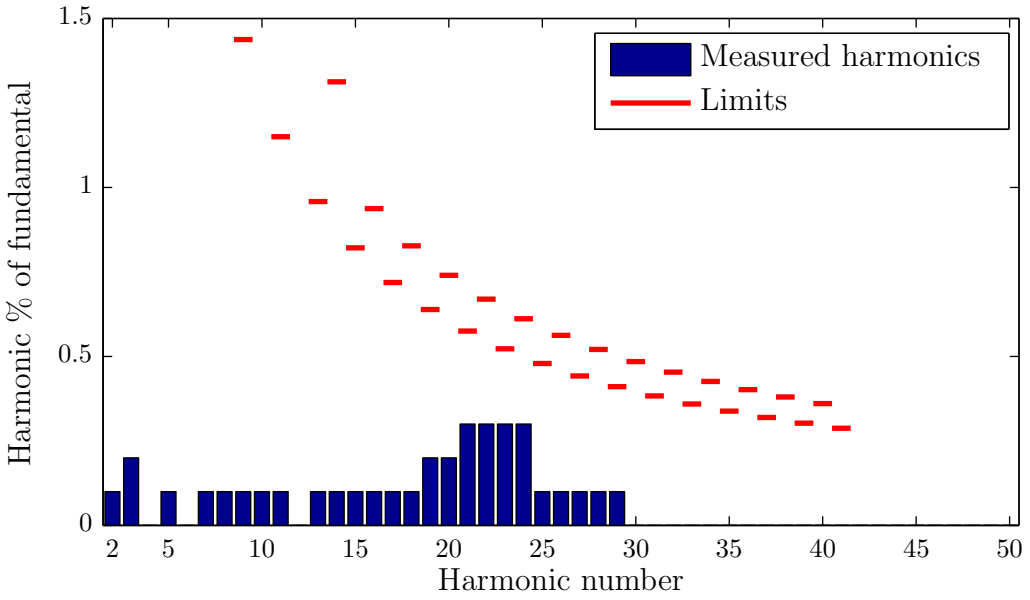


FIGURE 7.11: Harmonics of 16 A phase-to-neutral short-circuit current for hysteresis controller with $h_{lim} = \pm 1$ A and $C_f = 17\,\mu$F, and recalculated harmonic limits according to EN 61000-3-2. The shown harmonics, measured using a Fluke 734 power analyzer, are expressed as a percent of the fundamental (50 Hz). The measured THD is 0.7%.

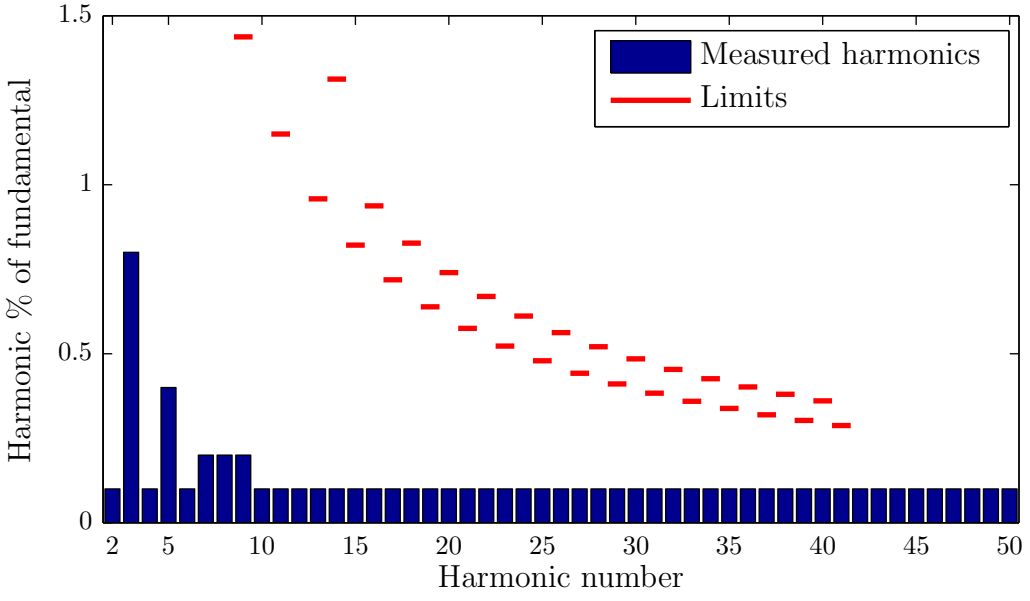


FIGURE 7.12: Harmonics of 16 A phase-to-neutral short-circuit current for PWM controller with $f_c = 11$ kHz and $C_f = 5\,\mu$F, and recalculated harmonic limits according to EN 61000-3-2. The shown harmonics, measured using a Fluke 734 power analyzer, are expressed as a percent of the fundamental (50 Hz). The measured THD is 1.1%.

7.4.2 Online short-circuit tests

Two experiments were designed to examine the behavior of a VISMA connected to the power network and operating in generator and motor modes when a network fault occurs. The goal of the first experiment was to show the response of the VISMA to a short-lasting grid fault and to show how it can contribute to the short-circuit current when operating in motor and generator modes. The goal of the second experiment was to show how the VISMA will behave if the grid fault persists for a longer time.

7.4.2.1 Short-lasting grid fault

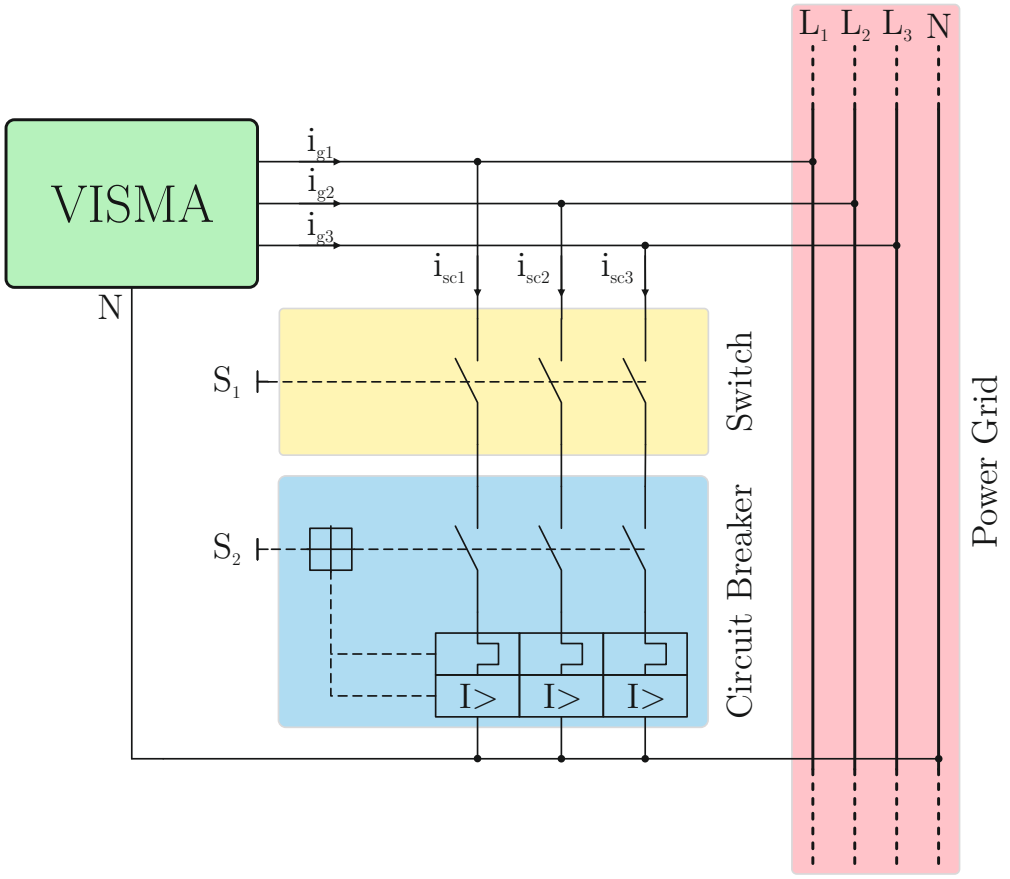


FIGURE 7.13: Experimental setup for creating a short-lasting grid fault

Figure 7.13 shows a schematic diagram of the experimental setup for creating a short-lasting symmetrical fault. A three-phase switch (S_1) is used to create a short circuit between the three supply phases and the neutral. This causes high short-circuit currents to flow through the switch (S_1) and circuit breaker (S_2),

causing the circuit breaker to trip and removing the short circuit. The duration of the short circuit depends on the properties of the circuit breaker. With the circuit breakers used in the experiments presented in this dissertation, the duration of the short circuit is approx. 2 ms. By observing the grid voltage and current during the short-lasting grid fault, we can make inferences about the effect of the VISMA on the power network.

Two scenarios must be examined. In the first scenario, the VISMA operates in generator mode feeding power into the grid when the short circuit occurs. Figure 7.14 plots the measured grid voltage and VISMA currents for this scenario for a single phase. When the grid fault occurs, the grid voltage drops, and the VISMA responds to this drop by increasing its output current.

In the second scenario, the VISMA operates in motor mode drawing power from the grid to charge its batteries. Figure 7.15 plots the grid voltage and VISMA currents for this scenario for a single phase. When the grid fault occurs, the grid voltage drops, and the VISMA responds by reducing the current drawn from the grid. If the polarity of the current is reversed because of the short circuit, the VISMA can supply a short-circuit current to the grid.

Operating in both generator and motor modes, the VISMA contributes to the short circuit current. In generator mode, the VISMA delivers the short circuit current directly by increasing its output current. The increase in current is, however, limited by the maximum output current of the inverter. In motor mode, the VISMA contributes to the short-circuit current by reducing the current drawn from the grid, allowing other generators in the power network to deliver more current to the short circuit. Also in motor mode, a short circuit can cause the polarity of the VISMA current to change, in which case the VISMA will supply the short circuit current directly.

A VISMA operating in motor mode can have a greater contribution to the short-circuit power than a VISMA operating in generator mode. E.g. a VISMA with a 16 A current rating feeding a 8 A into the grid can only increase its current output by 8 A during a short circuit. On the other hand, the same 16 A-rated VISMA operating in motor mode and drawing a 16 A current from the grid can, during a short circuit, reduce the drawn current and even supply a current of up to 16 A to the grid.

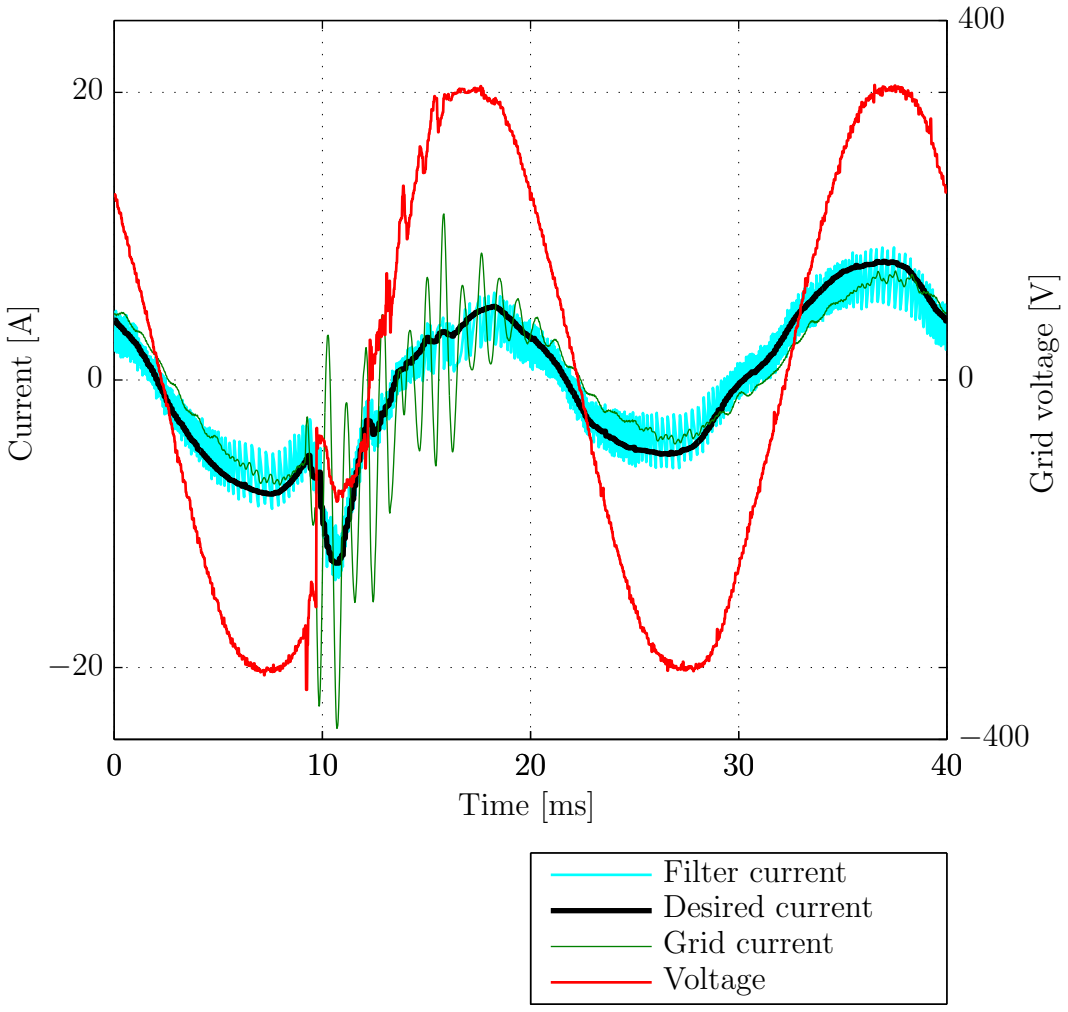


FIGURE 7.14: Measured grid voltage and VISMA currents in generator mode during short-lasting symmetrical short circuit fed in using a hysteresis current controller, shown for a single phase. When the short circuit occurs and the grid voltage drops, the current fed into the grid by the VISMA increases.

In both motor and generator modes we can observe that the filter current i_f, which is measured and used as feedback by the hysteresis current controller, tracks the desired current well. However, the grid current i_g is excited by the sudden surge in the current caused by the short circuit and begins to oscillate until it is eventually damped. This is similar to exciting the LCL filter with a step function. Putting a resistor in series with the filter capacitors may reduce the amplitude of this oscillation, but will lead to increased power losses in the inverter and a reduced filtering effect of the LCL filter under normal operating conditions.

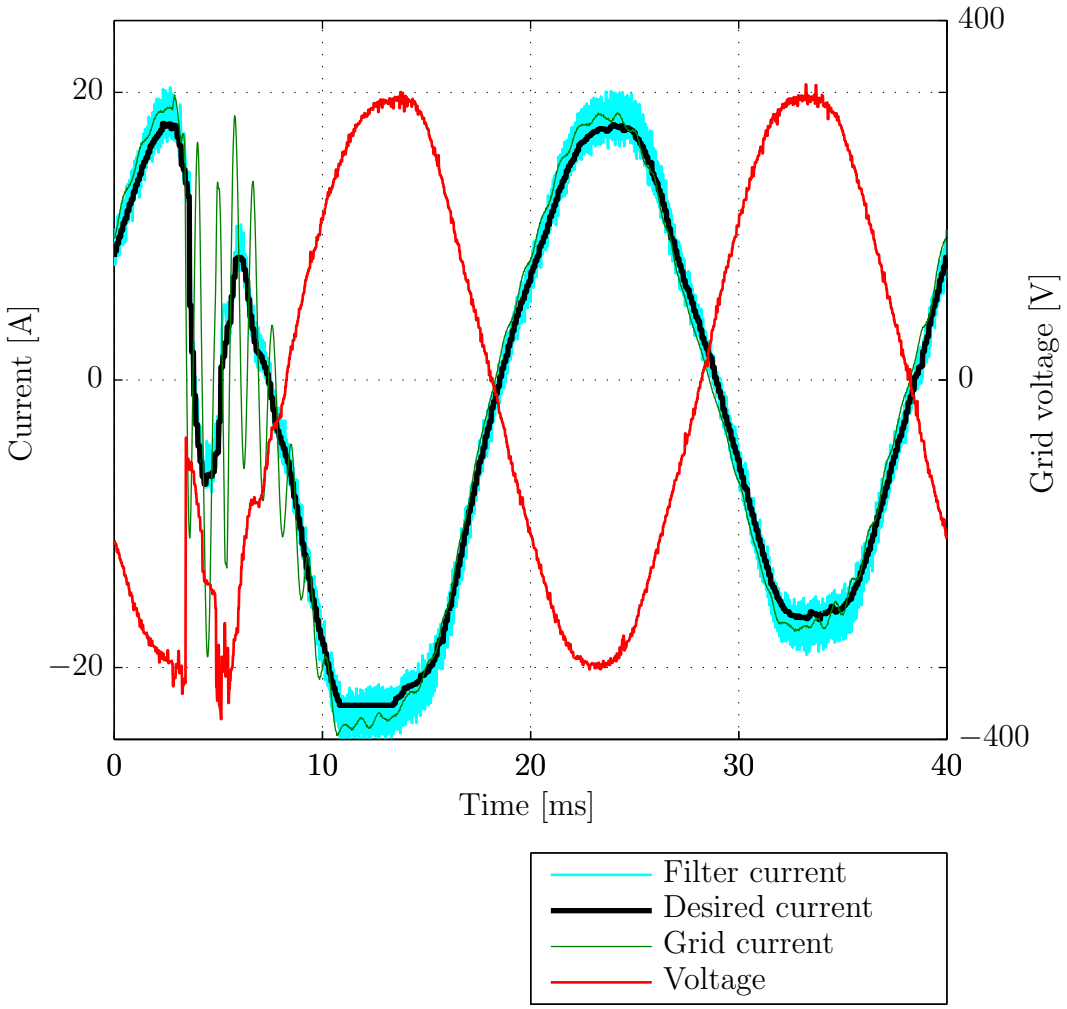


FIGURE 7.15: Grid voltage and VISMA currents in motor mode during short-lasting symmetrical short circuit fed in using hysteresis current controller, shown for a single phase. When the short circuit occurs and the grid voltage drops, and the current drawn by the VISMA declines.

7.4.2.2 Long-lasting grid fault

A schematic diagram for the experimental setup for generating a long-lasting symmetrical grid fault is shown in Figure 7.16. A three-phase switch (S_1) is used to create a short-circuit between the three supply phases and the neutral. This causes high short-circuit currents to flow through the switch (S_1) and circuit breaker (S_2). The circuit breaker is installed between the power grid and the VISMA. The high short-circuit current will cause the circuit breaker to trip and isolate the faulty part of the grid, leaving the VISMA short-circuited and disconnected from the grid. The short circuit causes the grid voltage to drop close to zero. According

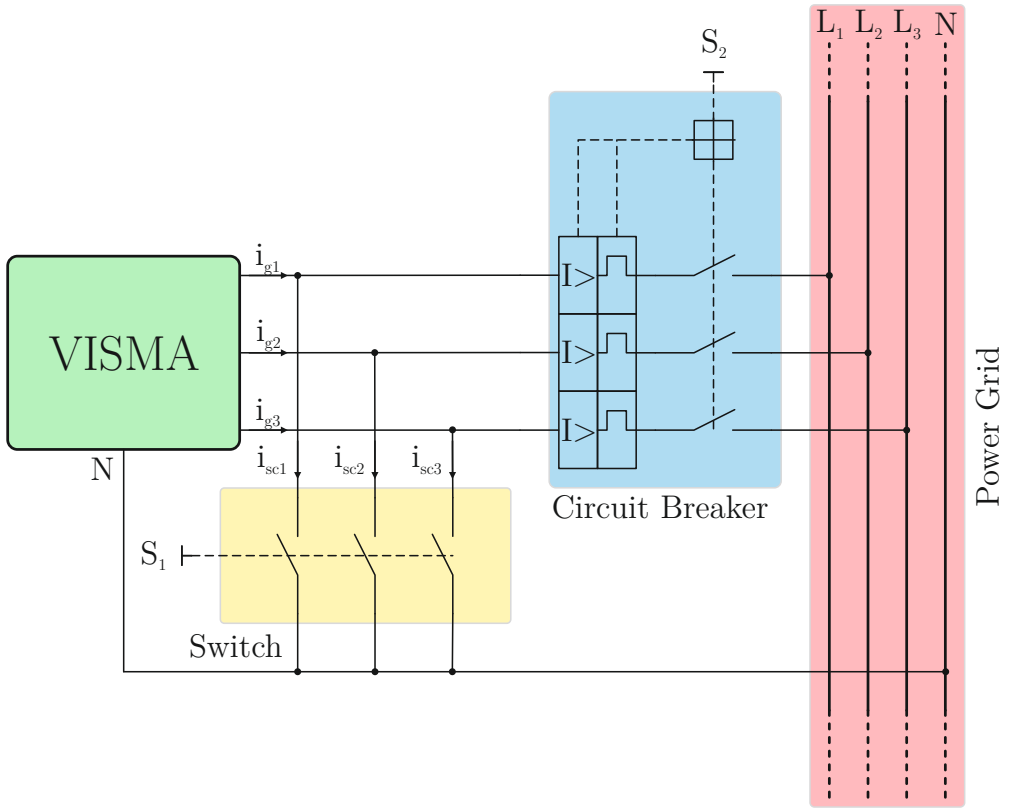


FIGURE 7.16: Experimental setup for creating a grid fault leaving the VISMA short-circuited and disconnected from the power grid

to the middle voltage guideline [57], which was used as a specification reference, if the grid voltage drops below 30% of the nominal value, a generator should stay connected to the grid for at least 150 ms (7.5 periods in a 50 Hz system) and be able to provide a short-circuit current.

Under normal operating conditions, the virtual synchronous machine is synchronized with the grid. With the grid voltage gone, the torque acting on the rotor will cause the rotor to accelerate, and, after some time, synchronism with the grid will be lost. If a longer short circuit occurs, the machine must disconnect from the grid and undergo resynchronization prior to reconnection.

In the experimental setup, the VISMA software was programmed to monitor the grid voltage and the angular frequency of the rotor, ω. If the RMS grid voltage drops below 30% of the nominal value for more than 10 periods, the virtual torque acting on the VISMA rotor is set to zero, and a control command is sent to the FPGA to switch off the IGBTs, effectively disconnecting the VISMA from the grid.

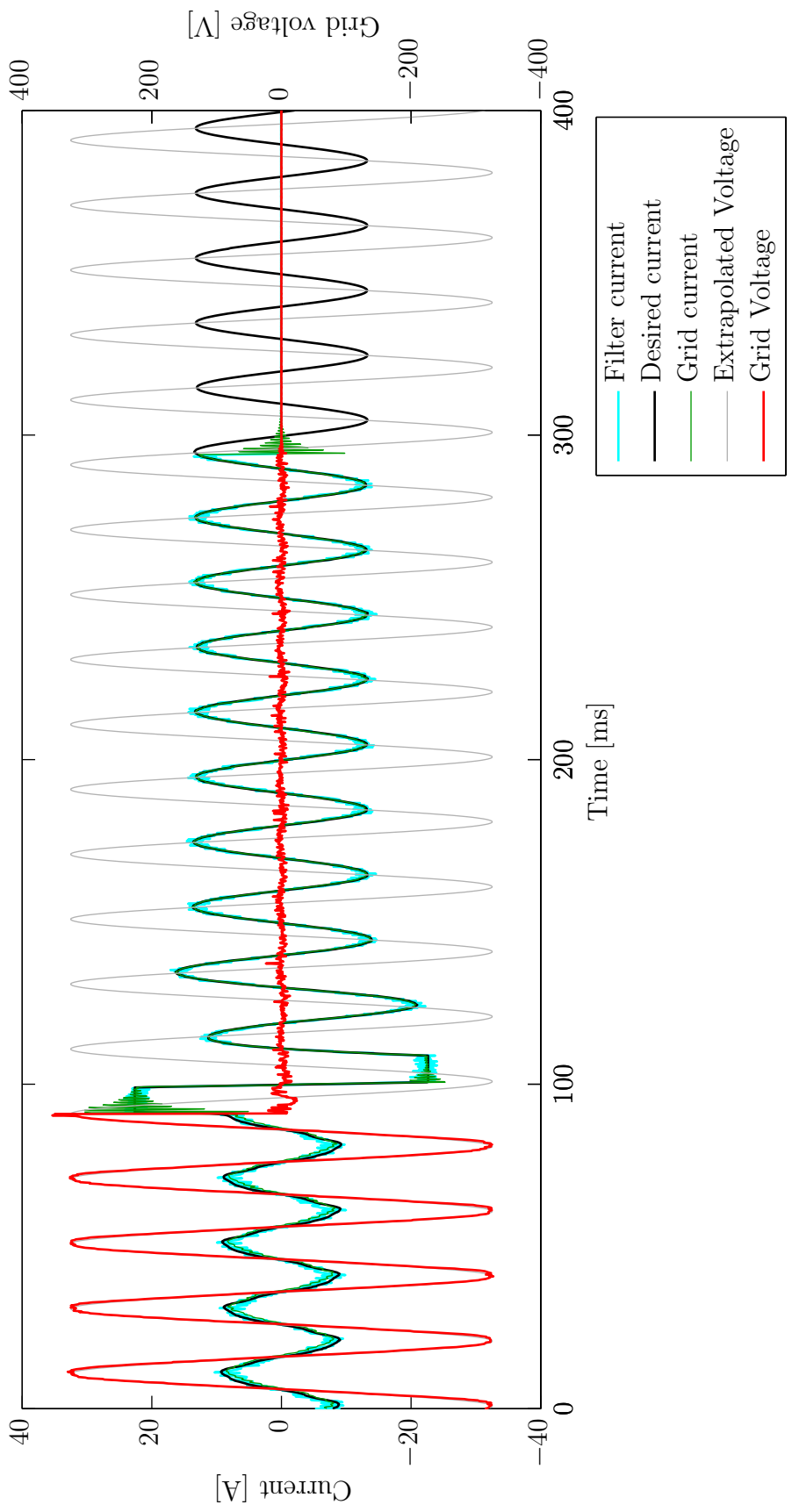


FIGURE 7.17: Short circuit at $t \approx 90\,\text{ms}$ for VISMA in generator mode. The VISMA delivers a short-circuit current for 10 periods of the voltage before disconnecting. The VISMA currents lag the extrapolated grid voltage.

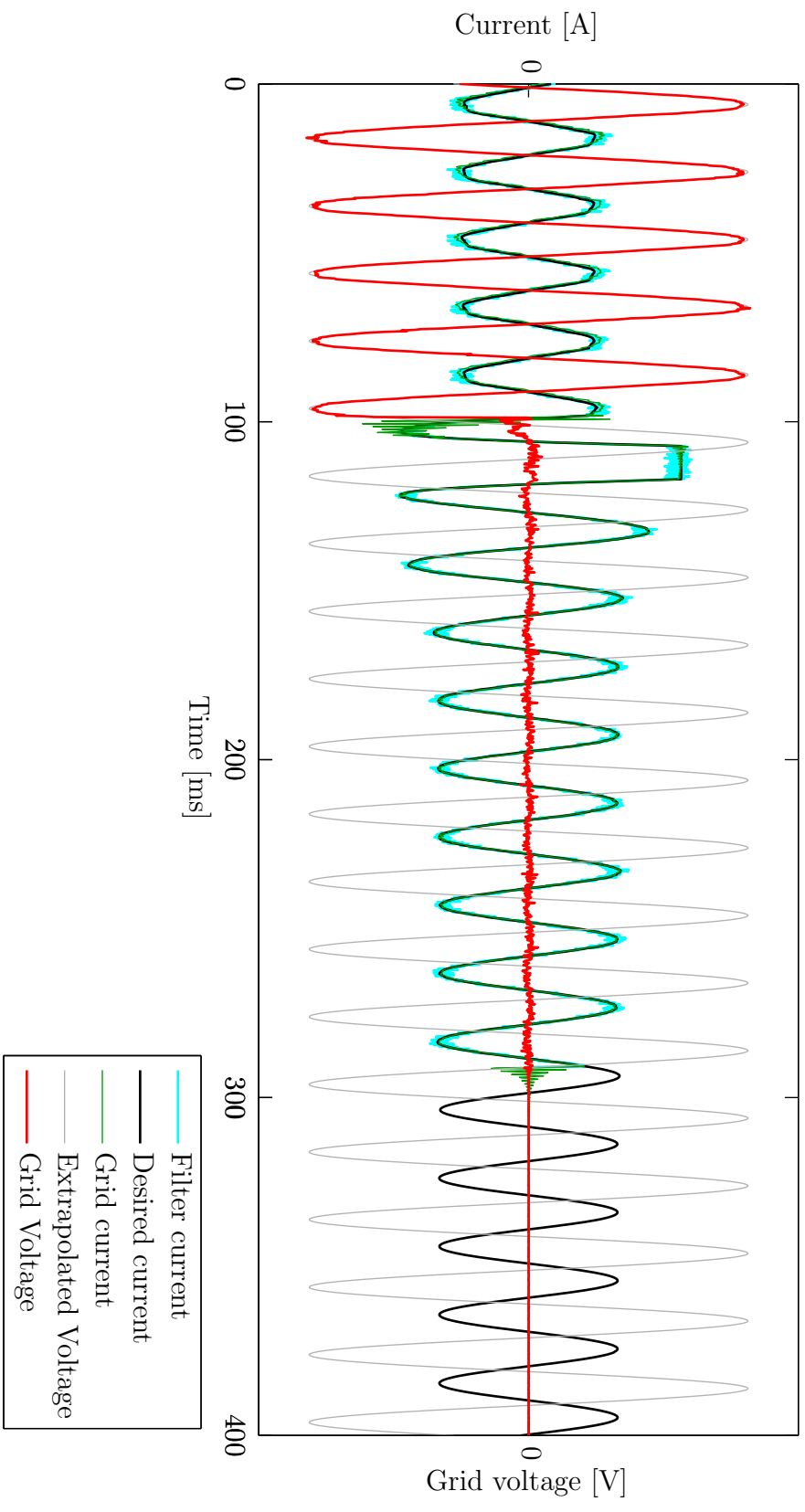


FIGURE 7.18: Short circuit at $t \approx 100$ ms for VISMA in motor mode. The VISMA delivers a short-circuit current for 10 periods of the the voltage before disconnecting. The VISMA currents lag the extrapolated grid voltage.

Two scenarios are considered in the experiments, one for the VISMA operating in motor mode and the other one for the VISMA operating in generator mode. In both scenarios, a hysteresis current controller is used to feed in the currents.

Figure 7.17 plots the measured grid voltage and VISMA currents for a single phase of the VISMA operating in generator mode. When the grid fault occurs at time $t \approx 90\,\text{ms}$, the measured voltage drops to around zero, and the VISMA responds with a very large current which exceeds the current rating of the inverter. The desired current is clipped at 22.63 A, which is equal to the amplitude of a current with an RMS value of 16 A. After the initial surge in the current, the VISMA continues to deliver a current lower than the peak current, but higher than the pre-fault current. If we were to extrapolate the grid voltage beyond the time when the short circuit occurred, as shown by the gray line in Figure 7.17, we would see that the short-circuit current lags the extrapolated grid voltage. Ten cycles of the voltage after the RMS voltage has dropped below 30% of the nominal value, the IGBTs are blocked, and the inverter stops feeding a current into the short circuit.

Figure 7.18 plots the grid voltage and VISMA currents for a single phase of the VISMA operating in motor mode when the short circuit occurs at $t \approx 100\,\text{ms}$. The short-circuit response is similar to the response in generator mode. After high initial transient currents, the VISMA delivers a short-circuit current to the grid which lags the extrapolated voltage.

Considering the tracking performance, we can see that the filter current follows the desired current set by the VISMA with little error. Also, the grid current starts to oscillate as a result of the sudden surge in the current caused by the short circuit.

7.4.3 PWM and hysteresis current controller performance during grid faults

Until now, the experimental results presented in this section were obtained using a hysteresis current controller to feed in the desired currents. In the online short-circuit experiments we observed that the grid current tends to oscillate for some time after the grid fault has occurred, not following the desired current (see green trace in Figures 7.14, 7.15, 7.17, and 7.18). In Chapter 6, hysteresis and PWM current controllers were compared, and based on experiments, a claim was made that using the PWM controller, it may be possible to feed in currents with less

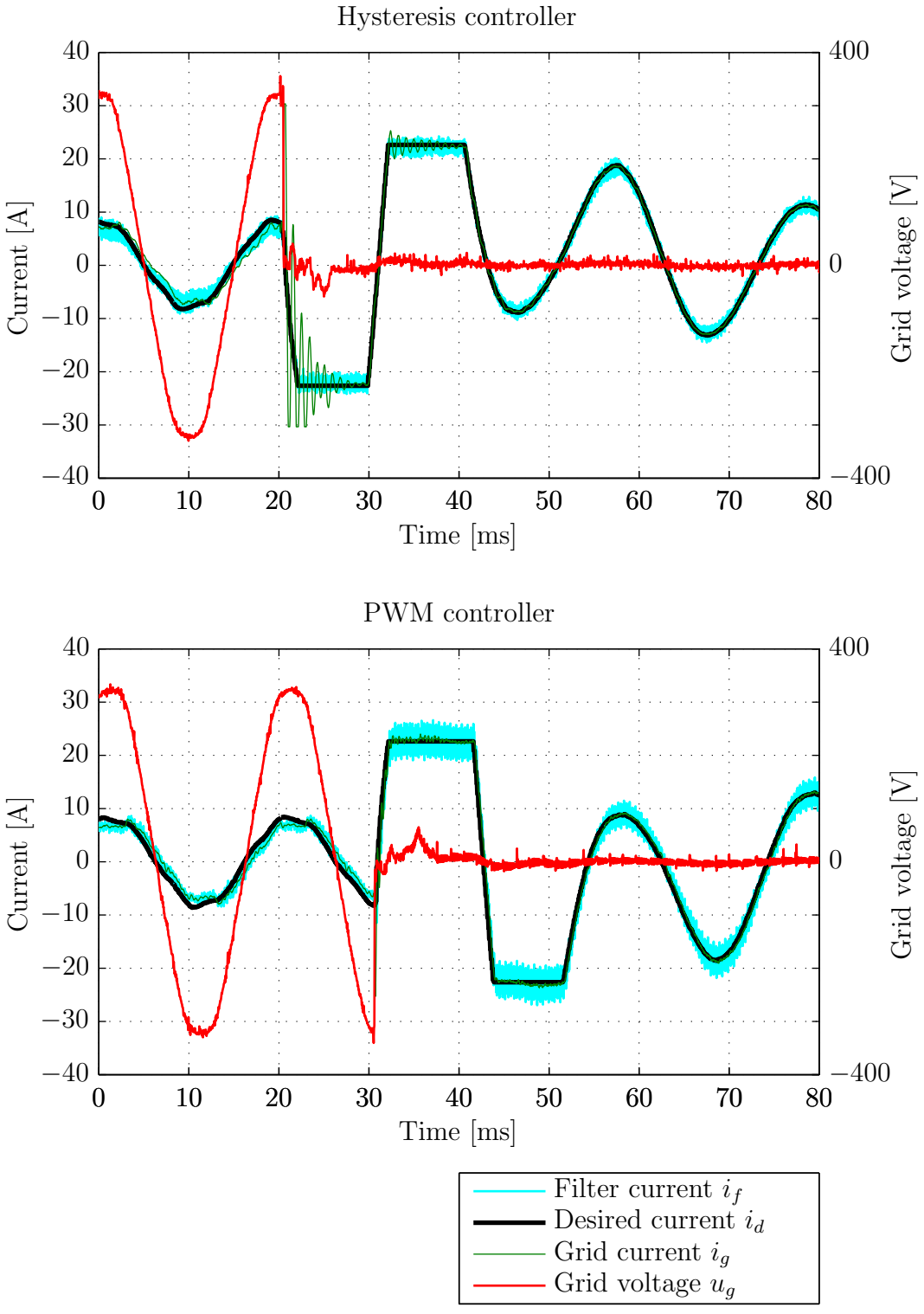


FIGURE 7.19: Currents fed into the grid using hysteresis controller (TOP) and PWM controller (BOTTOM) when long-lasting grid fault occurs. Using the PWM controller results in smaller oscillations of the grid current i_g. Clipping of the measured current occurs at 30 A (measurement limits).

overshoot and a faster settling time of the grid current i_g, as compared to the hysteresis controller. To further examine this claim, the short-circuit experiments were repeated using the PWM controller.

Figure 7.19 shows the results of an experiment where currents calculated using the VISMA are fed into the grid using a hysteresis current controller (TOP) and a PWM controller (BOTTOM) when a long-lasting short circuit occurs. The LCL filter configuration used in the experiment was $L_{fi} = 3\,mH$, $L_{fg} = 1\,mH$, and $C_f = 17\,\mu F$ for the hysteresis current controller and $L_{fi} = 3\,mH$, $L_{fg} = 1\,mH$, and $C_f = 5\,\mu F$ for the PWM controller. When the short circuit occurs and the grid voltage drops to zero, with both PWM and hysteresis controllers a surge of the grid current i_g occurs, but with the PWM current controller the oscillations are damped quicker and the current tracking is better.

Repeating the experiments multiple times, it could be observed that the magnitude of the oscillations depends on the instantaneous value of the grid voltage when the short circuit occurs. In most cases, the current tracking performance of the PWM current controller right after the short-circuit event is better than that of the hysteresis current controller.

7.5 Distant Grid Faults

In the previous section, the behavior of the VISMA was examined when the grid fault occurred near the VISMA, causing the grid voltage to drop to zero. In case of a distant short-circuit, the grid voltage measured at the VISMA will not drop to zero, but will sag, dropping below 90% of the nominal level. According to the middle voltage guideline [57], for voltage sags where the voltage stays above 30% of the nominal level, a generating unit is expected to stay connected to the grid for up to 1500 ms, depending on the grid voltage during the sag.

With our experimental setup, we were not able to create a long-lasting voltage sag in the grid. Instead, to test the response of the VISMA to a voltage sag, code was implemented in the VISMA software to make the machine model believe that the grid voltage had dropped to 75% of the nominal level by premultiplying all measured grid voltages with a factor of 0.75. The simulated voltage drop is maintained for 6 perdiods of the voltage (120 ms). We performed experiments with the VISMA operating in motor and generator modes. In the experiments,

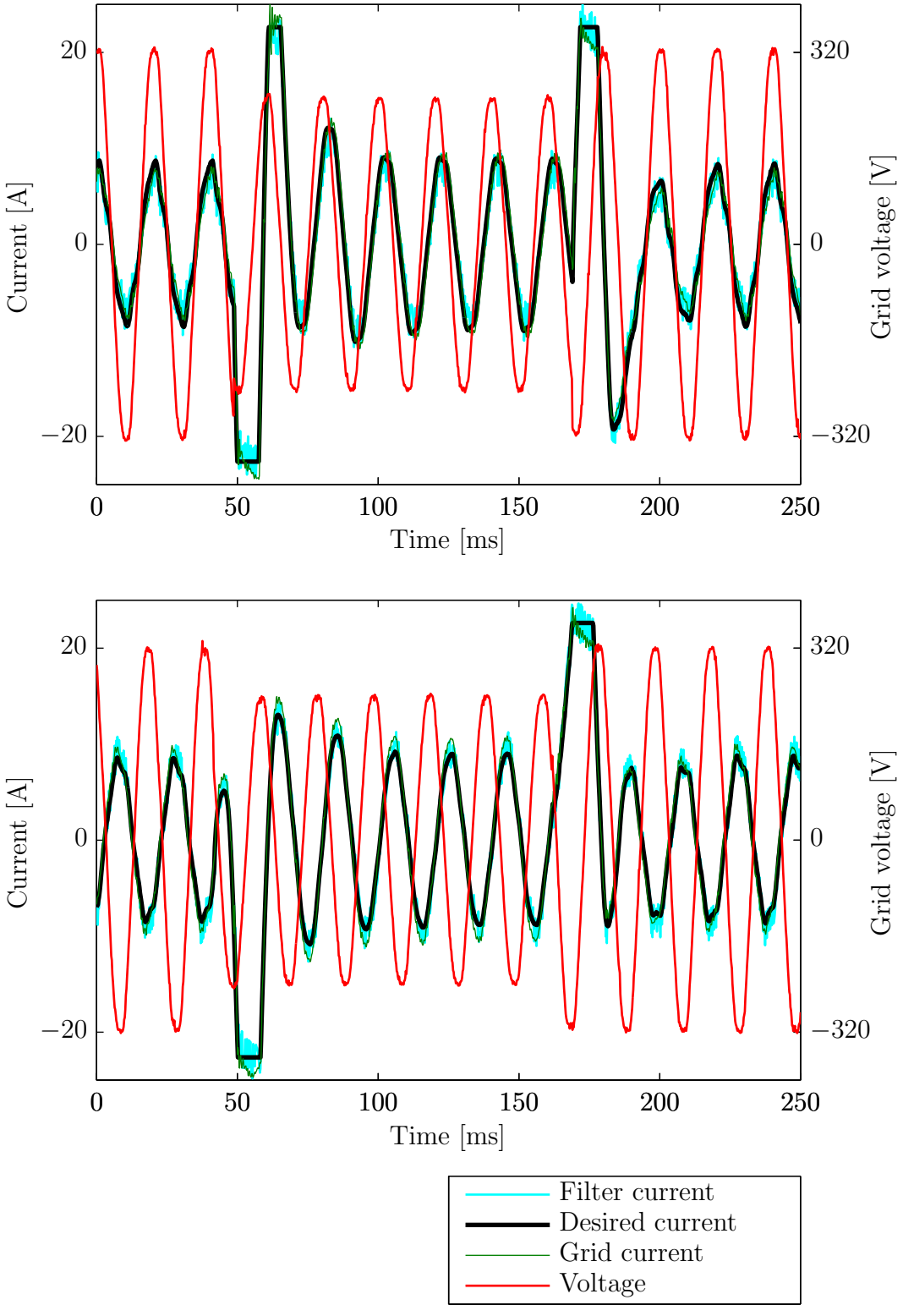


FIGURE 7.20: Response to voltage sag ($u_{\text{sag}} = 75\%\, u_n$) of the VISMA operating in generator mode (TOP) and motor mode (BOTTOM). During the sag, the VISMA delivers inductive reactive power, supporting the grid.

only the voltage drop is simulated. All other measurements presented within this section are actual measurements taken with the VISMA operating on the grid.

Figure 7.20 shows the measured currents on a single phase for a VISMA operating in generator mode (TOP) and in motor mode (BOTTOM) when the above-described simulated voltage drop occurs. In both motor and generator modes the sudden drop in voltage causes an initial surge in the current, which is clipped to the inverter's maximum current rating. After the initial surge, we can observe that the current lags the voltage, i.e. the VISMA is a supplier of inductive reactive power to the grid in both motor and generator modes.

7.6 Reconnection of the VISMA After a Grid Fault

A grid fault of sufficient duration will cause the VISMA to disconnect from the grid electrically by blocking all IGBTs in the inverter so no current can flow between the grid and the DC link. After the grid fault is removed, the VISMA can proceed with resynchronization and then with reconnection to the grid.

The machine model used in the VISMA is self-starting because of the damper windings present on the rotor, allowing it to start like an induction motor provided that the rotor inertia is sufficiently small. The rotor inertia of the synchronous machine is a parameter which can be chosen arbitrarily and can be modified during the operation of the VISMA without any adverse effect on the machine's behavior. Modifying the rotor inertia online is equivalent to attaching a rotating mass to the rotating rotor, both rotating at the same angular speeds.

Figure 7.21 shows a flowchart depicting the VISMA resynchronization process. When the machine is disconnected from the grid, the virtual mechanical torque is set to zero to prevent the rotor from accelerating, and the virtual inertia is set low to allow quick resynchronization. The virtual exciter voltage u_e is set to a level for which the desired currents set by the VISMA will be minimum. When the grid voltage is restored, the VISMA automatically synchronizes with the grid. If the grid voltage and angular frequency of the rotor are within specified limits for a preset amount of time, the virtual inertia can be increased, and resynchronization is considered complete. The IGBTs can then be switched on, and the virtual

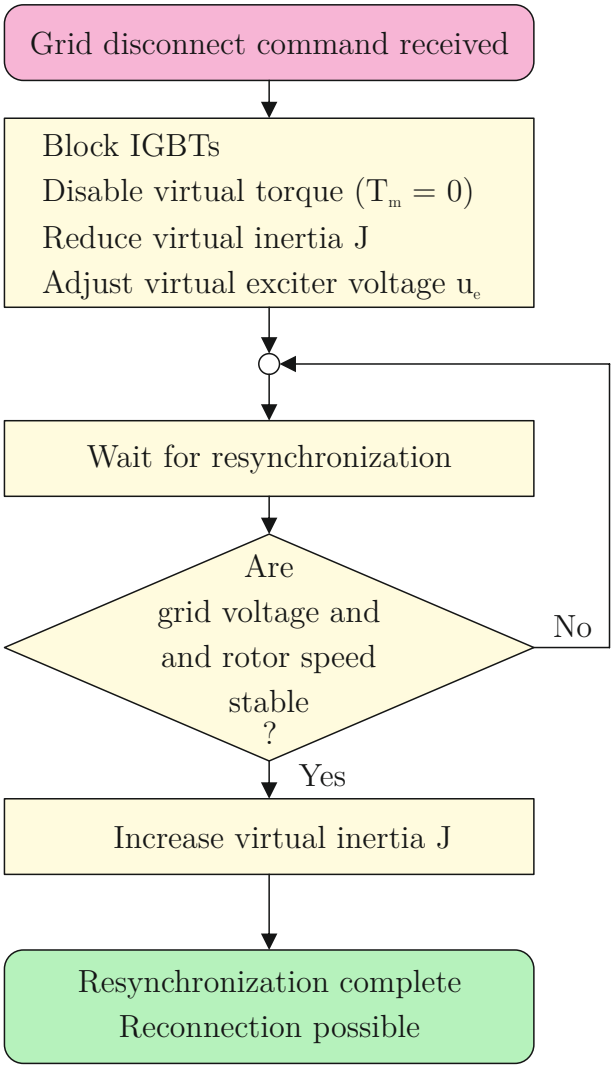


FIGURE 7.21: Flowchart representing the VISMA resynchronization process

mechanical torque T_m and virtual exciter voltage u_e gradually adjusted to provide the desired power output.

Chapter 8

Conclusions and Outlook

8.1 Conclusions

The Mobile VISMA presented in this dissertation presents a technological innovation which allows the integration of a VISMA system into a plug-in electric vehicle for use in V2G applications. It was shown that the real-time simulation of a synchronous machine can be performed on a low-cost 32-bit microprocessor with a 32-bit FPU using Euler's method for solving the machine differential equations, and that the machine model is stable even if the grid voltage measurements used as input to the machine model contain noise. Next, it was shown that a digital current controller for the VISMA can be implemented in FPGA. What this means is that the entire control electronics for the Mobile VISMA can be implemented on a single controller board using FPGA and microcontroller technologies. The same controller board can be used for controlling the traction motor of the electric vehicle, making the additional cost of installing VISMA technology in a vehicle minimal. Furthermore, the Mobile VISMA uses fewer parts and is easier to calibrate than previous VISMA versions. This reduces the production cost of the VISMA system and makes the FPGA-based Mobile VISMA architecture attractive for stationary applications as well.

The second problem dealt with in this dissertation was concerned with the quality of the currents fed into the grid by the FPGA-based current controller. Two different current controllers were implemented in FPGA, a hysteresis current controller and a PWM-based current controller, and the performance of these controllers

was tested and compared for different controller parameters and hardware settings. Both hysteresis and PWM current controllers were shown to be suitable for use with the VISMA system. The hysteresis current controller is simple to implement and only requires the measurement of the filter currents for feedback. The PWM-based controller is more sophisticated, and it only performs well when a grid-voltage compensator is used, which requires the measurement of the grid voltage and the use of a PWM inverter with a dead-time compensator. Experiments showed that the oscillations of the grid side current were smaller and were damped faster when using the PWM current controller.

The third problem was to investigate the behavior of the VISMA and current controllers during grid faults. The VISMA was designed to operate like a generator working on the middle-voltage level, allowing it to actively support the grid during power network faults. It was shown that both the PWM and hysteresis current controllers are capable of fault ride through and can be used to feed in a short-circuit current as high as the inverter's maximum current rating into the short circuit without causing interruptions or damage to the inverter hardware. The PWM controller performed better than the hysteresis current controller during network faults, producing smaller oscillations in the grid current and showing better current tracking performance than the hysteresis current controller. It was also shown that the VISMA will support the power grid during network faults regardless if it is operated in generator mode to feed power into the grid or in motor mode to charge the vehicle's batteries.

8.2 Outlook

On the grounds of the work presented in this dissertation, further research and development of the VISMA system are possible. One path to follow is the design of an integrated VISMA controller based on FPGA and microcontroller technologies, which, used to control an inverter, would give it VISMA functionality. This kind of controller board could be used for both stationary and mobile applications and would bring the VISMA closer to the market. Also, it would be interesting to investigate whether there are any commercially available inverters on which the VISMA could be implemented.

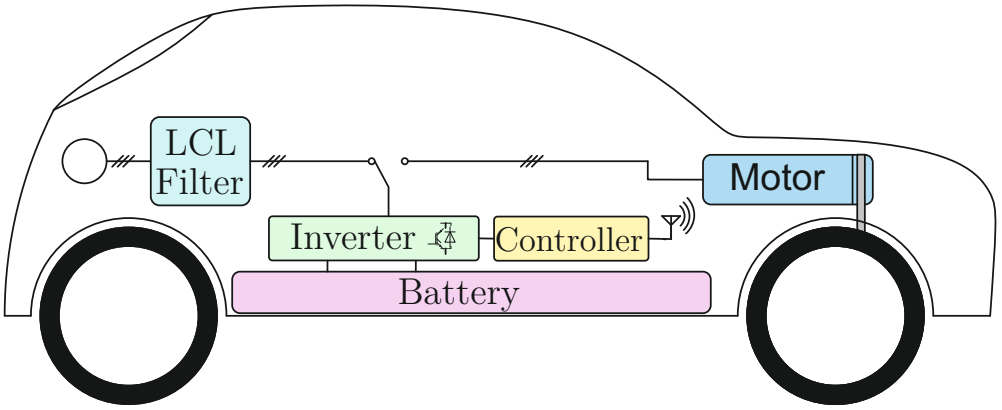


FIGURE 8.1: Future plug-in electric vehicle with Mobile VISMA. The inverter and FPGA-based controller are used for VISMA functionality during charging and for driving the electric motor.

The second path to follow is to further investigate the mobile applications of the VISMA system. In Figure 8.1 a concept of a future electric vehicle with the Mobile VISMA is presented. In this vehicle, the inverter and controller are used both for charging the vehicle batteries and supporting the power grid using VISMA technology while the car is connected to the grid, and for driving the electric motor while the vehicle is driven. In charging mode the VISMA can determine the state of the grid by measuring the grid voltage and frequency and adjust the charging rate to support the grid. It may also be possible for the power network operator to control the Mobile VISMA directly using a wireless connection with the controller, e.g. using 3G mobile technology. Both the design of V2G-capable vehicles with VISMA technology as well as the control of VISMA systems in these vehicles are interesting topics for future research.

List of Acronyms

ADC Analog-to-Digital Converter

DAC Digital-to-Analog Converter

CPU Central Processing Unit

DOD Depth of Discharge

EFZN Lower Saxony Energy Research Center

EMC Electromagnetic Compatibility

EMF Electromotive Force

ESR Effective Serial Resistance

FFT Fast Fourier Transform

FPGA Field Programmable Gate Array

FPU Floating Point Unit

IC Integrated Circuit

IEE Institute of Electrical Power Engineering

IGBT Insulated Gate Bipolar Transistor

IPM Intelligent Power Module

IPP Institute of Process and Production Control Technology

LiFePO4 Lithium Iron Phosphate

LPF Low-Pass Filter

MCU Microcontroller Unit

MIMO Multiple-Input and Multiple-Output

PCC Point of Common Coupling

PI Proportional Integral

PLECS Piece-wise Linear Electrical Circuit Simulation

PLL Phase-locked Loop

PWM Pulse Width Modulation

RMS Root Mean Square

SAE Sum of Absolute Errors

SOC State of Charge

SPI Serial Peripheral Interface

SPS Samples per Second

SSE Sum of Square Errors

THD Total Harmonic Distortion

UPS Uninterruptable Power Supply

V2G Vehicle to Grid

VDE Association of Electrical Engineering, Electronics, and Information Technology (*Verband der Elektrotechnik Elektronik Informationstechnik e.V.*)

VDEW German Electricity Association (*Verband der Elektrizitätswirtschaft e. V.*)

VHDL Very High Scale of Integration Hardware Description Language

VISMA Virtual Synchronous Machine

VSYNC Virtual synchronous machines for frequency stabilization in future grids with a significant share of decentralized generation

VSG Virtual Synchronous Generator

ZOH Zero-Order Hold

Appendix A

Experimental Setup

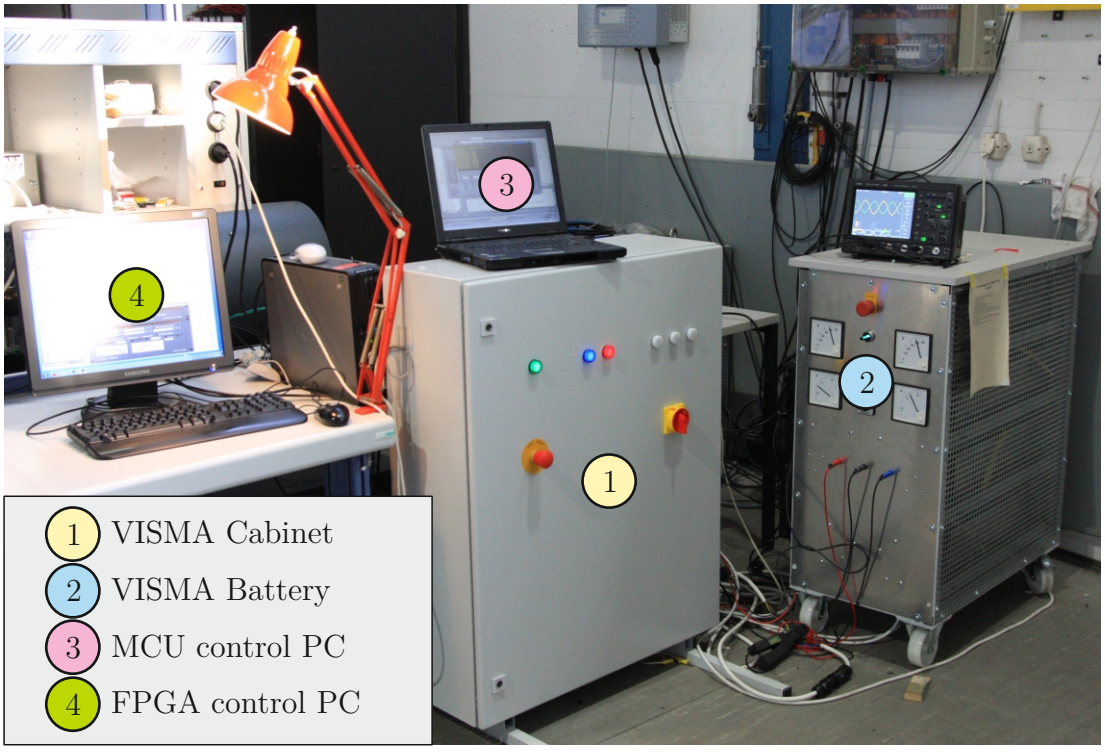


FIGURE A.1: Mobile VISMA experimental setup at the IEE

Figure A.1 shows the setup for the experiments with the Mobile VISMA. The experimental setup consists of the VISMA cabinet, the inside of which can be seen in Figure 3.1, a battery pack connected to the DC link, and a desktop and laptop PC for programming the FPGA and microcontroller, respectively, and controlling the VISMA system. The PC connected to the FPGA board also allows downloading

measurement data from the sensors installed in the VISMA cabinet using virtual instruments implemented in FPGA.

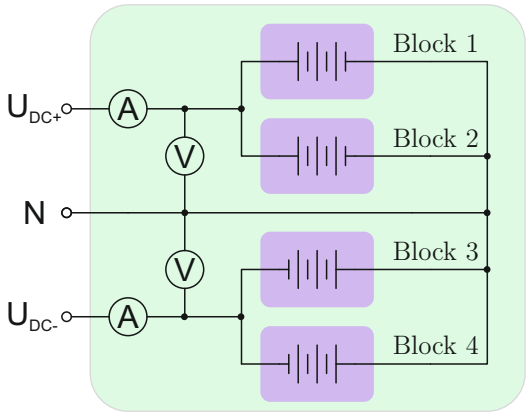


FIGURE A.2: Simplified schematic of VISMA battery pack. Each of the four battery blocks consists of 288 NiMH cells with a nominal voltage of 1.2 V.

A simplified schematic diagram of the battery pack used in the experiments is shown in Figure A.2. The battery pack consists of four battery blocks, each block comprising 288 NiMH cells with a nominal voltage of 1.2 V and a capacity of 6.2 Ah. Two blocks of cells each are connected in parallel to provide the positive and negative DC voltage, respecively. Connected this way, the battery pack has a nominal voltage of ±345 V. The maximum charge voltage of the battery pack is approx. ±400 V, and, according to the battery specifications, the capacity of the battery pack should be 12.4 Ah. However, the battery pack was made using second-hand batteries which were retired from use in a forklift and have a capacity smaller than originally specified. Using this battery pack for the experiments with the Mobile VISMA, care had to be taken to make sure that all experiments would be performed at the same SOC of the battery (same battery voltage) to make the results comparable.

Appendix B

FPGA Base Board

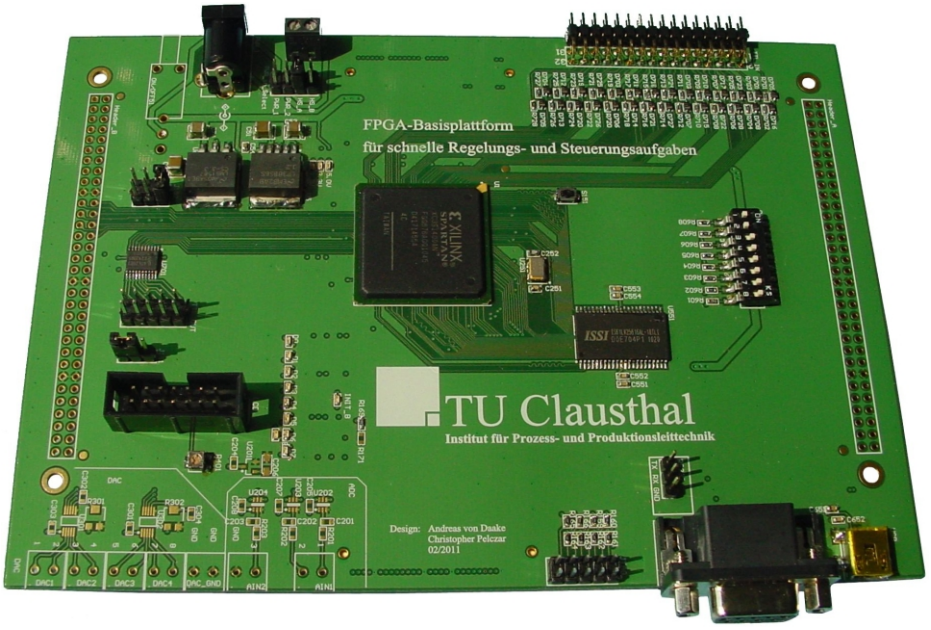


FIGURE B.1: The FPGA Spartan Baseboard developed at the IPP of the Clausthal Univeristy of Technology

Figure B.1 shows the IPP FPGA board that we developed with Andreas von Daake at the Institute of Process and Production Control Technology (IPP) [59]. The goal behind developing this board was to create a flexible and powerful FPGA-based controller platform for use in internal projects at the IPP. The custom-built FPGA board comprises a Spartan 3AN FPGA, SRAM, ADCs, Digital-to-Analog Converters (DACs), an RS232 and USB port, and multiple, multi-function I/O

ports, which can be used to interface with an external daughterboard through one of the headers or the high-speed data connector located on the bottom side of the PCB (not visible in figure). The IPP FPGA board can replace the Altium NanoBoard 3000 [23] development board used as the FPGA motherboard in the Mobile VISMA experimental setup and serve as a base for developing future FPGA-based VISMA systems. The Very High Scale of Integration Hardware Description Language (VHDL) code for the FPGA developed for the Mobile VISMA can be ported to the new hardware with ease, allowing the reuse of code developed for the current controllers, control of the ADCs, and protection functions.

Appendix C

Connection of Distributed Generators to the Grid – Standards

C.1 Harmonic current limits

The standards EN61000-3-2 [43] and EN61000-3-12 [44] describe limits for harmonic currents produced by equipment connected to public low-voltage systems for equipment with an input current $\leq$ 16 A, and $>$ 16 A and $\leq$ 75 A per phase, respectively. According to the VDE-AR-N 4105 application guide [42], generating facilities producing a nominal current $I_n < 16$ A should be treated as class-A devices under the EN61000-3-2 standard.

In the EN61000-3-2 standard, devices are grouped into one of four classes, depending on what influence they may have on the distribution network. These classes were established by taking into consideration how many of these devices are used, how long they are used, how many are used simultaneously, how much power they consume, and their harmonic spectrum. Class-A devices are the largest group, containing all equipment which are not portable tools and non-professional arc-welding tools (class B), lighting equipment (class C), or personal computers,

Harmonic Order n	**Harmonic limit [A]**
Odd harmonics	
3	2.30
5	1.14
7	0.77
9	0.40
11	0.33
13	0.21
$15 \leq n \leq 39$	$0.15 \cdot 15/n$
Even harmonics	
2	1.08
4	0.43
6	0.30
$8 \leq n \leq 40$	$0.23 \cdot 8/n$

TABLE C.1: Harmonic limits for class-A devices according to EN61000-3-2 [43]

monitors, or TV sets (class D). The harmonic limits for class-A devices are given in Amperes and are summarized in Table C.1.

C.2 Generation facilities connected to the low-voltage distribution network

The application guide VDE-AR-N 4105 [42], which was published in August 2011, is the new guideline describing the technical requirements for the connection and parallel operation of generators connected to the low-voltage distribution network and aims at improving stability and reliability of low-voltage distribution networks with a growing penetration of distributed generation. VDE-AR-N 4105 replaces the old German Electricity Association
(*Verband der Elektrizitätswirtschaft e. V.*) (VDEW) guideline described in [60].

The new guideline addresses the 50.2 Hz problem [61] by frequency dependent regulation of the active power and requires the generating facilities to be able to participate in static voltage maintenance by providing or consuming reactive power [42].

A programmable protection relay should be used to disconnect the facility within 200 ms if the grid voltage drops below 80% of the nominal voltage ($U_g < 0.8\,U_n$), or if the grid voltage exceeds the nominal voltage by 10% ($U_g > 1.1\,U_n$). The programmable protection relay should also disconnect the facility if the grid frequency drops below 47.5 Hz or exceeds 51.5 Hz. The programmable protection relay is therefore similar to the disconnection device described in VDE 0126-1-1 [62], which was used in devices made according to the VDEW guideline [60], but has different disconnection settings.

The VDE-AR-N 4105 guideline also provides a method for assessing whether the generating facility can be connected to the low-voltage network based on the parameters of the network and generating facility. Should the connection of the generation facility to the low-voltage network not be possible for technical reasons, the generation facility can be connected to the middle-voltage network provided it can meet the requirements of the middle-voltage guideline [57].

Bibliography

[1] Lisias V. L. Abreu and Mohammad Shahidehpour. Wind Energy and Power System Inertia. In *Power Engineering Society General Meeting*, 2006.

[2] Ralf Hesse. *Virtuelle Synchronmaschine*. PhD thesis, Clausthal University of Technology, June 2007.

[3] Hans-Peter Beck and Ralf Hesse. Virtual Synchronous Machine. In *9th International Conference on Electrical Power Quality and Utilization*, October 2007.

[4] J. Driesen and K. Visscher. Virtual synchronous generators. In *Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century, 2008 IEEE*, pages 1 –3, july 2008.

[5] K. Visscher and S.W.H. De Haan. Virtual synchronous machines (VSGs) for frequency stabilisation in future grids with a significant share of decentralized generation. In *SmartGrids for Distribution, 2008. IET-CIRED. CIRED Seminar*, pages 1 –4, june 2008.

[6] V. Van Thong, A. Woyte, M. Albu, M. Van Hest, J. Bozelie, J. Diaz, T. Loix, D. Stanculescu, and K. Visscher. Virtual synchronous generator: Laboratory scale results and field demonstration. In *PowerTech, 2009 IEEE Bucharest*, pages 1 –6, 28 2009-july 2 2009.

[7] M. Albu, K. Visscher, D. Creanga, A. Nechifor, and N. Golovanov. Storage selection for DG applications containing virtual synchronous generators. In *PowerTech, 2009 IEEE Bucharest*, pages 1 –6, 28 2009-july 2 2009.

[8] T.V. Van, K. Visscher, J. Diaz, V. Karapanos, A. Woyte, M. Albu, J. Bozelie, T. Loix, and D. Federenciuc. Virtual synchronous generator: An element of future grids. In *Innovative Smart Grid Technologies Conference Europe (ISGT Europe), 2010 IEEE PES*, pages 1 –7, oct. 2010.

[9] M. Albu, J. Diaz, V. Thong, R. Neurohr, D. Federenciuc, M. Popa, and M. Calin. Measurement and remote monitoring for virtual synchronous generator design. In *Applied Measurements For Power Systems (AMPS), 2010 IEEE International Workshop on*, pages 7 –11, sept. 2010.

[10] Qing-Chang Zhong and George Weiss. Synchronverters: Inverters that Mimic Synchronous Generators. *IEEE Transactions on Industrial Electronics*, 58, April 2011.

[11] M. Torres and L.A.C. Lopes. Frequency control improvement in an autonomous power system: An application of virtual synchronous machines. In *Power Electronics and ECCE Asia (ICPE ECCE), 2011 IEEE 8th International Conference on*, pages 2188 –2195, 30 2011-june 3 2011.

[12] K. Sakimoto, Y. Miura, and T. Ise. Stabilization of a power system with a distributed generator by a virtual synchronous generator function. In *Power Electronics and ECCE Asia (ICPE ECCE), 2011 IEEE 8th International Conference on*, pages 1498 –1505, 30 2011-june 3 2011.

[13] Yong Chen, R. Hesse, D. Turschner, and H.-P. Beck. Improving the grid power quality using virtual synchronous machines. In *Power Engineering, Energy and Electrical Drives (POWERENG), 2011 International Conference on*, pages 1 –6, may 2011.

[14] K. Clement-Nyns, E. Haesen, and J. Driesen. The impact of charging plug-in hybrid electric vehicles on a residential distribution grid. *Power Systems, IEEE Transactions on*, 25(1):371 –380, feb. 2010.

[15] E. Sortomme and M.A. El-Sharkawi. Optimal charging strategies for unidirectional vehicle-to-grid. *Smart Grid, IEEE Transactions on*, 2(1):131 –138, march 2011.

[16] Mcdavis A. Fasugba and Philip T. Krein. Gaining vehicle-to-grid benefits with unidirectional electric and plug-in hybrid vehicle chargers. In *Vehicle Power and Propulsion Conference (VPPC), 2011 IEEE*, pages 1 –6, sept. 2011.

[17] André Haubrock. *Degradationsuntersuchungen von Lithium-Ionen Batterien bei deren Einsatz in Elektro- und Hybridfahrzeugen.* PhD thesis, Clausthal University of Technology, June 2011.

[18] Christopher Pelczar, Markus Stubbe, Dirk Turschner, and Oliver Zirn. Mobile Virtual Synchronous Machine for V2G Applications. In *17th World Congress on ITS*, 2010.

[19] Markus Stubbe. Programmierung, Aufbau und Inbetriebnahme einer Vituellen Synchronmachine (VISMA). Master's thesis, Clausthal University of Technology, 2008.

[20] TriCore TC1796 32-Bit Single Chip Microcontroller Datasheet. Infineon Technologies AG, 2005.

[21] Paul C. Krause, Oleg Waynczuk, and Scott D. Sudhoff. *Analysis of Electric Machinery and Drive Systems.* IEEE Press, John Wiley & Sons, 2 edition, 2002.

[22] Joe D. Hoffmann. *Numerical Methods for Engineers and Scientists.* McGraw Hill, 2 edition, 1992.

[23] Altium Nanoboard 3000 Series Datasheet. Altium Ltd., 2009.

[24] Spartan-3AN FPGA Family Data Sheet. Xilinx Inc., 2011.

[25] TriBoard TC1796 Hardware Manual. Infineon Technologies AG, 2005.

[26] Current Transducer LA 50-S/SP1 Datasheet. LEM Holding SA.

[27] AD7367 True Bipolar Input, Dual 14-bit, 2-channel, Simultaneous Sampling SAR ADC Datasheet. Analog Devices, .

[28] AD7682/AD7689 16-Bit, 4-Channel/8-Channel, 250 kSPS PulSAR ADC Datasheet. Analog Devices, .

[29] ADuM1400/ADuM1401/ADuM1402 Quad-Channel Digital Isolators Datasheet. Analog Devices, Inc.

[30] Felix Jenni and Dieter Wüest. *Steuerverfahren für selbstgeführte Stromrichter*, chapter 3, pages 49–50. vdf Hochschulverlag AG an der ETH Zürich und B.G Teubner Stuttgart, 1995.

[31] Verband der Netzbetreiber VDN e.V. Technische Regeln zur Beurteilung von Netzrückwirkungen. 2007.

[32] Heinz Zenker, Alexander Gerfer, and Bernhard Rall. *Trilogy of Inductors*. Würth Elektronik eiSos GmbH & Co. KG, 3rd edition.

[33] 60MBP50RA120 R-Series IGPT-IPM Datasheet. Fuji Electric Co.,Ltd.

[34] IDXP630 Inverter Interface and Digital Deadtime Generator for 3-Phase PWM Controls Datasheet. IXYS Corporation, 1998.

[35] Dezentrale Netzqualittsverbesserung in Niederspannungsnetzen mit virtuellen Synchronmaschinen – EFRE-Projekt W2-80025696. TU Clausthal & Inensus GmbH, 2008-2011.

[36] Entwicklung einer virtuellen Synchronmaschine fr den Einsatz in unterbrechungsfreien Stromversorgungen – EFRE-Projekt W2-80025699. TU Clausthal & Inensus GmbH, 2008-2011.

[37] Piece-wise Linear Electrical Circuit Simulation User Manual. Plexim GmbH, 2010.

[38] Ulrich Tietze, Christoph Schenk, and Eberhard Gamm. *Electronic Circuits – Handbook for Design and Application*. Springer, 2 edition, 2008.

[39] AN2007-04 - How to calculate and minimize the dead time requirement for IGBTs properly. Infineon Technologies AG, 2007.

[40] FS50R12KE3 IGBT Module Techinical Information. Infineon Technologies AG, 2002.

[41] FS50R12W2T4 IGBT Module Techinical Information. Infineon Technologies AG, 2009.

[42] VDE-AR-N 4105, *Erzeugungsanlagen am Niederspannungsnetz - Technische Mindestanforderungen für Anschluss und Parallelbetrieb von Erzeugungsanlagen am Niederspannungsnetz*. VDE Verband der Elektrotechnik Elektronik Informationstechnik e.V., 2011.

[43] EN 61000-3-2, *Electromagnetic Compatibility (EMC) - Part 3-2: Limits for harmonic currents emissions (equipment input current* $\leq$ $16\,A$ *per phase)*. DIN Deutsches Institut für Normung e.V. and VDE Verband der Elektronik and Informationstechnik e.V., 2005.

[44] EN 61000-3-2, *Electromagnetic Compatibility (EMC) - Part 3-2: Limits for harmonic currents produced by equipment connected to public low-voltage systems with input current* $>$ $16\,A$ *and* $\leq$ $75\,A$ *per phase* . DIN Deutsches Institut für Normung e.V. and VDE Verband der Elektronik and Informationstechnik e.V., 2004.

[45] Fluke 434/435 Three Phase Power Quality Analyzer User Manual. Fluke Corporation, 2010.

[46] WaveJet 300A Oscilloscopes Datasheet. Lecroy Corporation, 2006.

[47] A621, A622 Current Probes Datasheet. Tektronix Inc., 2011.

[48] J. Love. *Process automation handbook: a guide to theory and practice*. Springer, 2007.

[49] Oliver Zirn, Christian Vetter, and Karl-Heinz Sauermann. *Automatisierungstechnik im Maschineningenieurwesen*. Papierflieger Verlag GmbH, 1 edition, 2011.

[50] Dämpfungsoptimale Reglereinstellung an Servoachsen – DFG-Projekt ZI-1301-1/1. TU Clausthal & Universtiät Marburg, 2010-2013.

[51] Oliver Zirn. *Machine Tool Analysis – Modelling, Simulation and Control of Machine Tool Manipulators - A Habilitation Thesis*. Department of Mechanical & Process Engineering, ETH Zurich, May 2008.

[52] Ashok Kumar. *Control Systems*. McGraw Hill, 2006.

[53] Jong-Lik Lin. A New Approach of Dead-Time Compensation for PWM Voltage Inverters. *IEEE Transactions on Circuits and Systems*, 49, April 2002.

[54] Charles Gross. *Electric Power Engineering Handbook*, chapter Fault Analysis in Power Systems. CRC Press, 2 edition, 2007.

[55] Mohamed E. El-Hawary. *Electrical Energy Systems*. CRC Press, 2000.

[56] Jerry C. Whitaker. *AC Power Systems Handbook*, chapter Power System Components. CRC Press, 2 edition, 1999.

[57] Bundesverband der Energie-und Wasserwirtschaft. Richtlinie für Anschluss und Parallelbetrieb von Erzeugungsanlagen am Mittelspannungsnetz. June 2008.

[58] Verband der Netzbetreiber VDN e.V. beim VDEW. Transmissioncode 2007 - Netz- und Systemregeln der deutschen Übertragungsnetzbetreiber. August 2007.

[59] Andreas von Daake and Christopher Pelczar. FPGA Basisplattform für schnelle Regelungs- und Steuerungsaufgaben. Technical report, Faculty of Mathematics/Computer Science and Mechanical Engineering, Clausthal University of Technology, 2011.

[60] Verband der Netzbetreiber VDN e.V. beim VDEW and Verband der Elektrizitätswirtschaft VDV e.V. Energieerzeugungsanlagen am Niederspannungsnetz. August 2001.

[61] Jens Bömer, Karsten Burges, Pavel Zolotarev, and Joachim Lehner. Impact of Large-scale Distributed Generation on Network Stability During Over-Frequency Events & Development of Mitigation Measures – Summary. Ecofys Germany GmbH and the University of Stuttgart, September 2011.

[62] *Automatic Disconnection Device Between a Generator and the Public Low-Voltage Grid*, February 2006. DIN V VDE V 0126-1-1:2006-02.